WD9710 Fully Integrated 64-Bit Graphics and Motion Video Accelerator Data Book

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1.0 INTRODUCTION

This document introduces and describes the Western Digital® WD9710 Fully Integrated 64-bit Graphics and Motion Video Accelerator (hereinafter referred to as the WD9710 accelerator) for all desktop applications.

The WD9710 provides uncompromised graphics and video performance through acceleration, integration, 64-bit architecture, and motion video processing.

Uncompromised graphics performance and TV-quality full screen motion video are brought together for the first in a single device in Western Digital's new WD9710. Western Digital has developed the WD9710 to provide the highest level of performance for the Microsoft Windows Family, IBM's OS/2, SCO's Unix and DOS-based Graphical User Interface (GUI) applications.

The WD9710 incorporates a high-performance, pipelined, 64-bit architecture throughout the graphics and motion video engines. A 320 MB/s DRAM display memory interface supplies the 64-bit graphics and motion video pipeline with the data rates needed to process two 32-bit per pixel operations per clock cycle. To provide further functionality, performance, and cost savings a full 24-bit RAMDAC and programmable clock synthesizer have been integrated into the WD9710. Adding these architectural features to glueless 32-bit interfaces for both VESA-VL and PCI systems buses provides the user with the ultimate in flexible, value-added performance.

The WD9710 surpasses other 64-bit graphics-only solutions on the market by fully integrating motion video acceleration into one part. With the WD9710, the burden of motion video processing and display has been off-loaded from the processor or external specialty hardware. This is accomplished in the motion video engine with built-in logic for YUV to RGB color space conversion, scaling and interpolation, shared frame buffer control for a co-processor interface, chroma-key, and motion video data stream input via the PCI bus or VAFC port. The end result is that the WD9710 provides the mainstream with performance, functionality, and integration where it is needed most - for multimedia playback of true color motion video at 30 frames per second in VGA and SVGA formats.

Western Digital realizes the importance of software in today's display controller environment. Western Digital has developed and provides support for a wide range of enhanced display drivers for high-quality and high-resolution applications. Besides the industry standard operating systems listed above, extensive effort has been placed in motion video processing and CODEC acceleration including MPEG, Cinepak, and Indeo. Making software more user-friendly has been achieved in the WD9710 with simplified driver installation and setup, Intel's Plug and Play interface support, and VESA's DDC-1 and DDC-2 smart monitor control.

Green PC power savings is a must for a complete display subsystem. The WD9710 has full support and hardware control for all the DPMS monitor modes. Along with DPMS, the WD9710 also has the ability to reduce memory clocks and power down the internal RAMDAC, clock synthesizer, and portions of the digital logic.

Western Digital offers customers a total solution with proven hardware performance, extensive software driver support, and unequaled BIOS compatibility. Available for the WD9710 is a manufacture package for VESA-VL or PCI bus interfaces. This greatly reduces research and design cycles - saving the developer money. These packages give the developer a complete, proven solution to guarantee reduced time to market with less expense and more confidence.

1.1 FEATURE HIGHLIGHTS

1.1.1 Graphics Engine

- True 64-bit Architecture allows up to 320 MB/s of data throughput
- Support 24-bit true color acceleration of resolutions up to 1024 by 768
- Maximum resolution of 1600 by 1200 at 256 colors
- Hardware BITBLT for 8, 16, and 24-bit color modes
  - Pattern, rectangle, trapezoidal fill
  - Raster operations
  - Full 32-bit memory or I/O port transfers to or from host
  - Transparency
- Hardware Cursor
  - 64 by 64 or 32 by 32 pixels
  - Two and three color modes
  - Inversion and transparency
- Hardware line draw using Bresenham or Strip Line Algorithms

1.1.2 Motion Video Engine

- Single graphics and motion video display memory via single frame buffer architecture
- Intelligent storage of motion video data in on-screen or off-screen memory based on occluding requirements
- Color space conversion from multiple YUV formats, including the standard 4:1:1 or 4:2:2 CCIR 601, to RGB format
- Proprietary, area-weighted algorithm for horizontal and vertical scaling and interpolation from 0% to 800%
- VESA Advanced Feature Connector (VAFC) supported with a 16-bit motion video port
- Standard feature connector support
- External video source genlock capability
- Hardware-assisted CODEC Acceleration and Support
  - MPEG-1 Collaborative Compression Architecture
  - Cinepak
  - Indeo

1.1.3 System Features

- Internal 135MHz, 24-bit, true color RAMDAC
- Internal programmable memory and pixel clock synthesizers
- Integrated, glueless support for PCI 2.0 and VESA-VL (50MHz) system interfaces
- 64-bit or 32-bit DRAM memory interface in a 1, 2, or 4M byte configuration
- Flexible memory price/performance through
  - 256K by 4, by 8, or by 16 DRAM configurations
  - Extended Data Out (EDO) support
  - Fast page and multiple CAS support
- Multiple level FIFO on host bus to allow zero wait state CPU cycles and PCI 2.0 burst mode support
- Programmable virtual memory addressing for CPU memory address space
- Green PC support via DPMS control and logic/PCLK/RAMDAC power management
- 208-pin MQFP package

1.1.4 Software Support

- Fully hardware accelerated Microsoft DCI provider/driver
- MPEG-1 CODEC provided as full MCI driver meeting open MPEG and OM-1 standards
- Custom accelerated Cinepak and Indeo CODECs available
- Software drivers available for Windows family, DOS, OS/2, and SCO/Unix
- User-configurable, VESA-compatible BIOS
- Full Plug and Play compatibility
- 100% VGA, EGA, CGA, MDA, and HGC compatible
- Oasis Configuration Application for
  - Installation
  - Graphics and Motion Video Setup
  - Power management control
- VESA compatibility for DDC-1 and DDC-2 "smart monitor" control
- Manufacturing test programs

1.2 ORDERING INFORMATION

The WD9710 is supplied in a 208-pin MQFP package. Use the following part number when ordering: **WD9710ZZ**

1.3 DOCUMENT SCOPE

The intent of this data book is to provide a detailed description of the WD9710. This data book should be used by hardware engineers designing video subsystems or by software engineers developing BIOS, drivers, utilities, or applications. Documentation and specifications of Western Digital developed BIOS, drivers, utilities and applications are published as separate documents.

In addition to this introduction to the WD9710, the following sections of this document provide a description of the WD9710 architecture and related interfaces, signal descriptions, internal register descriptions, application information for the graphics engine and motion video engine, timing information, and package dimensions.

Appendix A contains a list of reference documents that may be useful to users of this document.

Appendix B provides a change record for this document.

2.0 ARCHITECTURE

2.1 INTRODUCTION

The WD9710 contains the following internal modules:

- **System Features**
  - System Interface
  - Display Memory Controller
  - Internal Clock Generator
  - Internal RAMDAC
  - Power Management
  - Signature Analyzer
- **Drawing Engine**
  - Hardware Clipping
  - Hardware BITBLT
  - Vector Control
  - VGA Graphics Controller
- **Video Engine**
  - CRT Controller
  - VGA Sequencer
  - Serializer
- **Video Pipe**
  - Attribute Controller
  - Direct Indexed Color
  - Hardware Cursor
- **Motion Video Acceleration**
  - Motion Video Memory Control
  - YUV to RGB Color Space Conversion
  - Scaling and Interpolation Control
  - VESA Advanced Feature Connector (VAFC)

Each of these modules is described in the following sections and their interconnections are shown in Figure 2-1.

2.2 SYSTEM FEATURES

2.2.1 System Interface

The WD9710 System Interface provides the connections and buffering for interfacing to a VESA VL-Bus or PCI bus. Both the address bus and the data bus are 32-bits wide and there are discrete logic buffers to accommodate the control signals for each system bus type.

The PCI-bus interface is fully compliant with the PCI-bus revision 2.0 specification. The interface contains a multilevel FIFO that allows full PCI burst mode/write cache support. The WD9710 can be configured for a total glueless interface for either the PCI bus or the VESA VL-bus.

2.2.2 Display Memory Controller

The WD9710 operates with either a 32-bit or 64-bit DRAM interface. The WD9710 supports most types of DRAM, including 256K by 4 and 256K by 8 and 256K by 16 DRAMs and both dual-CAS and dual-WE types. The WD9710 fully supports fast page mode and Extended Data Out (EDO) memory modes.

2. 2.2.1 Memory Modes

The WD9710 supports 1, 2, or 4 megabytes of display memory in many configurations. The available resolutions include 640 by 480, 800 by 600, 1024 by 768, 1280 by 1024, and 1600 by 1200. Various color depths are available including 4, 8, 15, 16, and 24 bits per pixel. Display memory may contain indexed RGB, direct RGB, or YUV pixel color data. (Refer to Section 4 for additional information about memory modes.)

2. 2.2.2 Configuration Control

External pull-down resistors are used on the display memory data bus lines to control the configuration setup during power turn-on and system reset. These pull-down resistors determine the WD9710 status at start up (refer to Table 24-4).

2.2.3 Internal Clock Generator

The WD9710 incorporates an internal dual-clock generator that provides a display memory clock (MCLK) at 80 MHz maximum, and a video dot clock (VCLK) at 135 MHz maximum. Within their specified range, both generator outputs are fully programmable and are derived from the 14.318 MHz system clock that is available in the IBM PC/XT/AT, PS/2, and compatible computer systems. Either or both of the internal clocks can be turned off so that an external source may be used.

2.2.4 Internal/external RAMDAC

The WD9710 incorporates an internal RAMDAC with a pixel clock (PCLK) rate of up to 135 MHz.

The RAMDAC incorporates a 256 by 18 look-up table and is fully compatible with industry-standard operation (such as the Inmos IMSG176) while also supporting 15-bit, 16-bit, 24-bit, and 32-bit per pixel modes.

An external RAMDAC option is supported through an industry-standard interface.

2.2.5 Power Management

The WD9710 supports both chip and monitor power management. With a built-in activity detector and configurable timer, the WD9710 can control power-on (power-up) and power-off (power-down). For power-down operation, the monitor is signaled, via the DPMS protocol, to enter suspend mode. Internally, the WD9710 initiates a power-down of the whole device by switching MCLK and VCLK to their slowest frequencies and turning off the DAC portion of the RAMDAC palette and display memory.

In addition, the host processor, through software, can fully control the WD9710 power management features.

2.2.6 Signature Analyzer

An on-board signature analyzer eases verification of chip functionality and assures that only fully-functional WD9710 accelerators are shipped to customers.

2.3 DRAWING ENGINE

2.3.1 Clipping

Hardware clipping is provided that permits drawing engine updates only within a rectangular area of display memory.

2.3.2 Hardware BITBLT

A Hardware Bit Block Transfer (BITBLT) circuit copies rectangular regions of pixels between areas of display memory. All BITBLT functions are available including raster operations, plane masks, transparency, and scan fills.

Also, BITBLT operations can be performed to or from system memory with host assistance, with the WD9710 providing rotation and masking, as well as other BITBLT operations.

Monochrome to color expansion is also provided, including expansion to two-colors or to one color plus transparent.

2.3.3 Vector Control

The WD9710 is capable of drawing vectors, including Bresenham and strip vector lines, anywhere in display memory.

2.3.4 VGA Graphics Controller

The VGA Graphics Controller supports both standard VGA and extended register access to all VGA graphics functions.

2.4 VIDEO ENGINE

2.4.1 CRT Controller

The CRT Controller defines the horizontal and vertical timing of the WD9710. It also controls display scrolling, panning, text, and block cursor parameters.

2.4.2 VGA Sequencer

The VGA Sequencer supports both standard VGA and extended register access to all VGA sequencer functions.

2.4.3 Serializer

The Serializer controls how data is pixel interpreted in display memory and translated to the video output.

2.5 VIDEO PIPE

2.5.1 Attribute Controller

The Attribute Controller supports VGA attributes with both standard VGA and extended register access.

2.5.2 Direct Indexed Color

Direct Indexed Color provides a register block that supports a special 8-bit direct-indexed color mode. When operated in this mode the RGB (3-3-2) color is color-corrected for more precise control of the red, blue, and green intensities.

2.5.3 Hardware Cursor

A hardware cursor is incorporated to provide a cursor of up to 64 by 64 pixels. The cursor provides either three colors, or two color plus inversion. The cursor operates smoothly over the graphics and video windows.

2.6 MOTION VIDEO ACCELERATION

The WD9710 architecture supports accelerated motion video processing. The acceleration includes motion video memory control, YUV color space conversion, motion video scaling and interpolation, and support for the VESA Advanced Feature Connector (VAFC).

2.6.1 Motion Video Memory Control

Motion video data, decompressed by a CODEC in the CPU or by external hardware, can be stored in on-screen or off-screen display memory. Storing the motion video data in on-screen or off-screen display memory can cause performance differences for both motion video acceleration and graphics acceleration. The WD9710 and its software drivers determine the best storage method for video motion data based upon requirements of the application program.

Motion video data can be stored in either YUV or RGB format. However, since True color YUV data requires fewer bits-per-pixel, the WD9710 memory controller intermixes YUV and RGB data in display memory to provide the best use of memory. BITBLT operations are provided to transfer the motion video data to display memory.

2.6.2 YUV to RGB Color Space Conversion

The internal YUV to RGB color space conversion is obtained by implementing the CCIR 601 recommended algorithms. The WD9710 supports the following standard data formats:

- YUV (4:2:2)
- YUV (4:1:1)

Additionally, the WD9710 supports several packed YUV formats along with custom YUV formats for MPEG, CINEPAK, and INDEO.

When motion video data is sent to the RAMDAC for display, YUV data is converted to the RGB format.

2.6.3 Scaling and Interpolation Control

The WD9710 provides motion video scaling and interpolation control in both the horizontal and vertical directions. Scaling and interpolation allows the best use of memory space while providing the highest level of performance. For the vertical range, a Discrete Differential Algorithm (DDA) is used to provide non-integral scaling from 0 to 800%. Horizontal scaling and interpolation uses a proprietary hardware assisted algorithm to provide interpolation in a range of 0 to 800% in non-integral steps. Horizontal and vertical scaling are fully independent.

2.6.4 VESA Advanced Feature Connector (VAFC)

The WD9710 supports the baseline VAFC specification, by accepting 16-bit digital video data. The digital video data is then combined with graphic and other motion video data at the RAMDAC level. For additional information about the VAFC connector, refer to Section 24.7.

The WD9710 architecture has reserved connector pins and registers for implementing a direct write to the frame buffer with access to all motion video acceleration features.

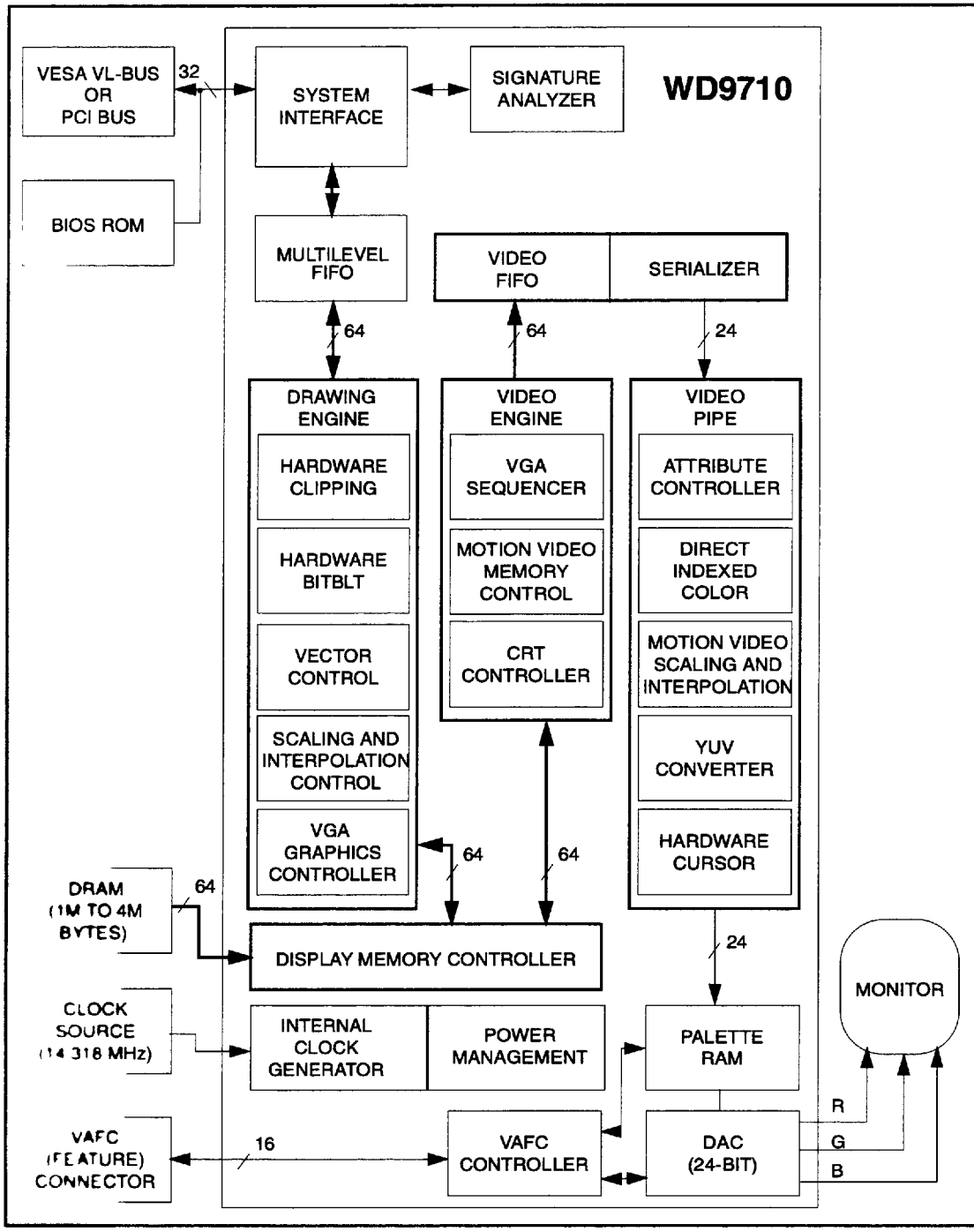


FIGURE 2-1. WD9710 SYSTEM BLOCK DIAGRAM

3.0 INTERFACES

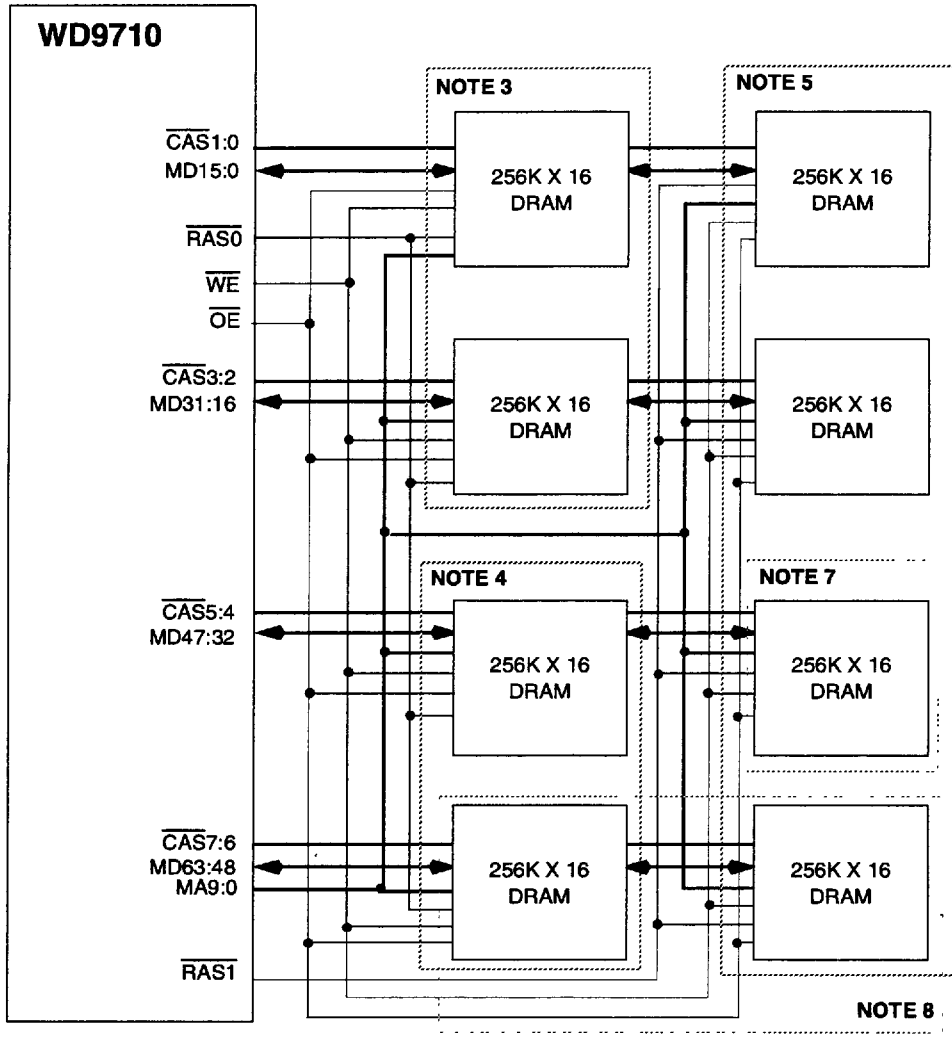
The WD9710 incorporates interfaces for the VESA VL-bus and PCI bus. The PCI bus interface is multiplexed and does not require external logic components. The VL-bus interface can be multiplexed or de-multiplexed, although the de-multiplexed interface is available only without external RAMDAC or VAFC port support. Using the de-multiplexed interface requires fewer external board components.

3.1 OVERVIEW

The following sections provide typical interface diagrams for the WD9710. These diagrams are intended to provide an example and may not include all of the discrete components used in many actual designs.

Combinations of host interface and memory interface design, other than the ones shown in this section, are possible.

3.2 DRAM INTERFACE



NOTES:

1. When only one bank is used, the $\overline{RAS0}$ and $\overline{RAS1}$ lines are driven with the same value.
2. For RAMs that use dual $\overline{WE}$'s, replace $\overline{CAS}$7:0 with $\overline{WE}$7:0 and replace $\overline{WE}$1:0 with $\overline{CAS}$1:0.
3. The minimum configuration is 1M byte in two DRAMs.
4. The 2M byte configuration uses four DRAMs as shown for notes 3 and 4.
5. A 4M byte configuration uses all eight DRAMs.
6. Four 256K x 4 DRAMs can be used in place of any 256K x 16 DRAM.
7. Two 512K x 8 DRAMs can be used in place of any 256K x 16 DRAM.
8. Two 256K x 8 DRAMa can be used in place of any 256K x 16 DRAM.

FIGURE 3-1. DRAM INTERFACE

3.3 PCI BUS INTERFACE

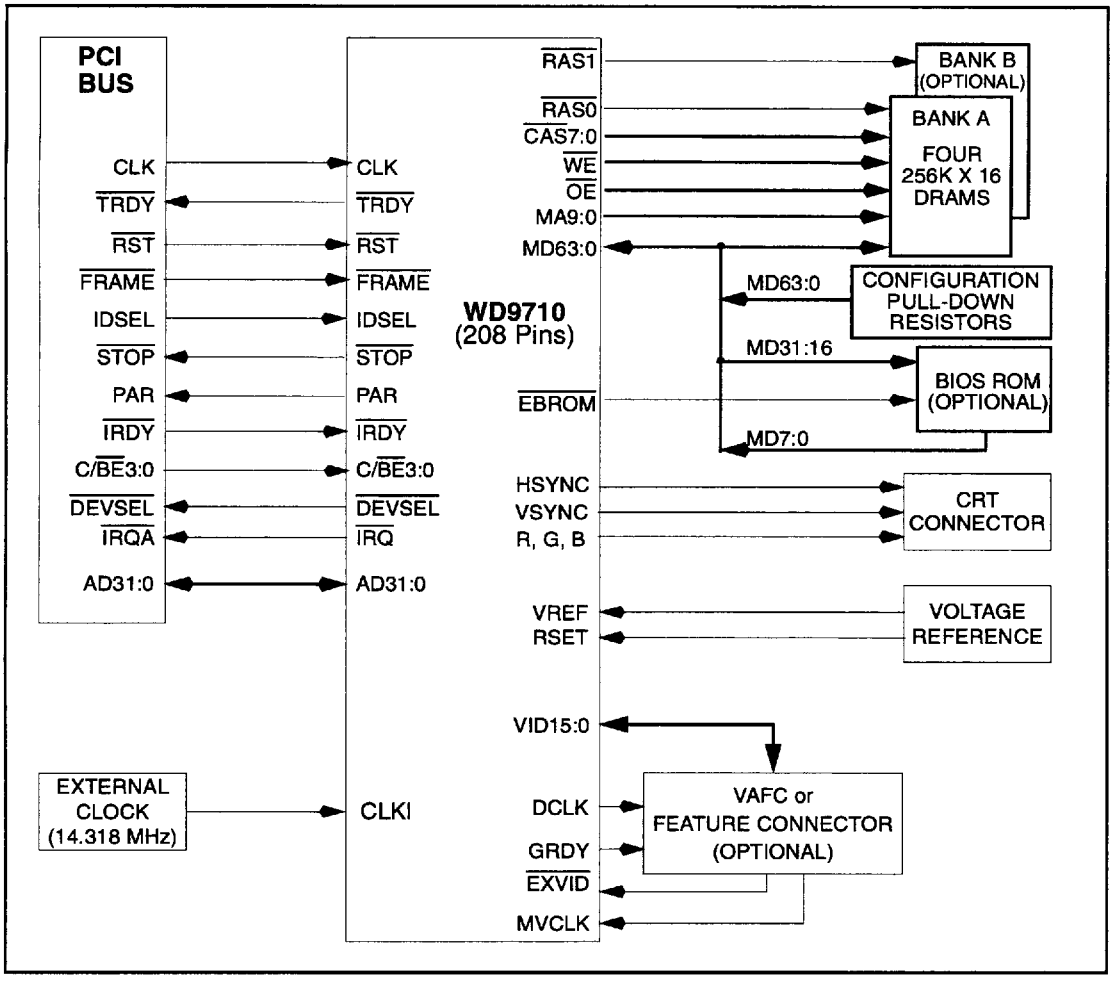


FIGURE 3-2. PCI BUS INTERFACE

3.4 MULTIPLEXED VL-BUS INTERFACE

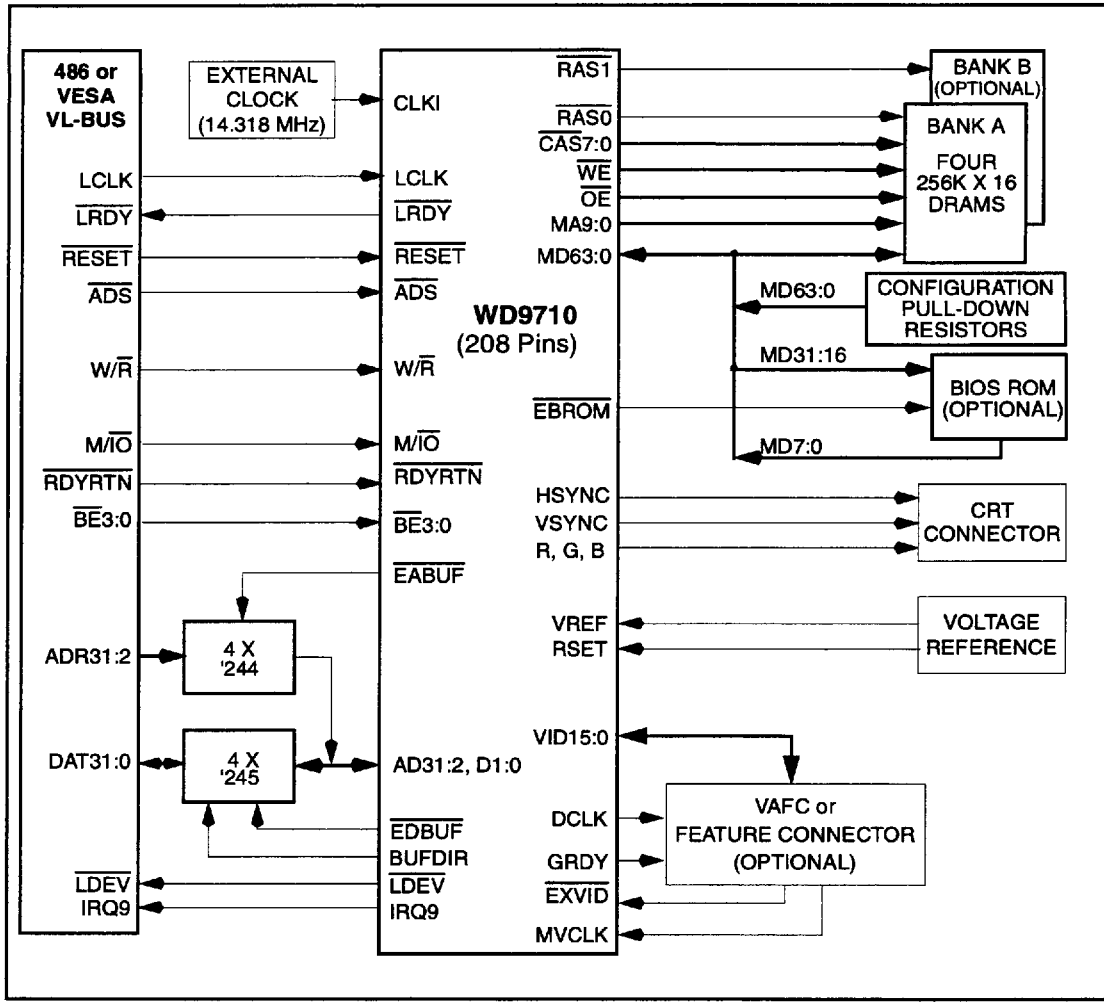


FIGURE 3-3. MULTIPLEXED VL-BUS INTERFACE

3.5 DE-MULTIPLEXED VL-BUS INTERFACE

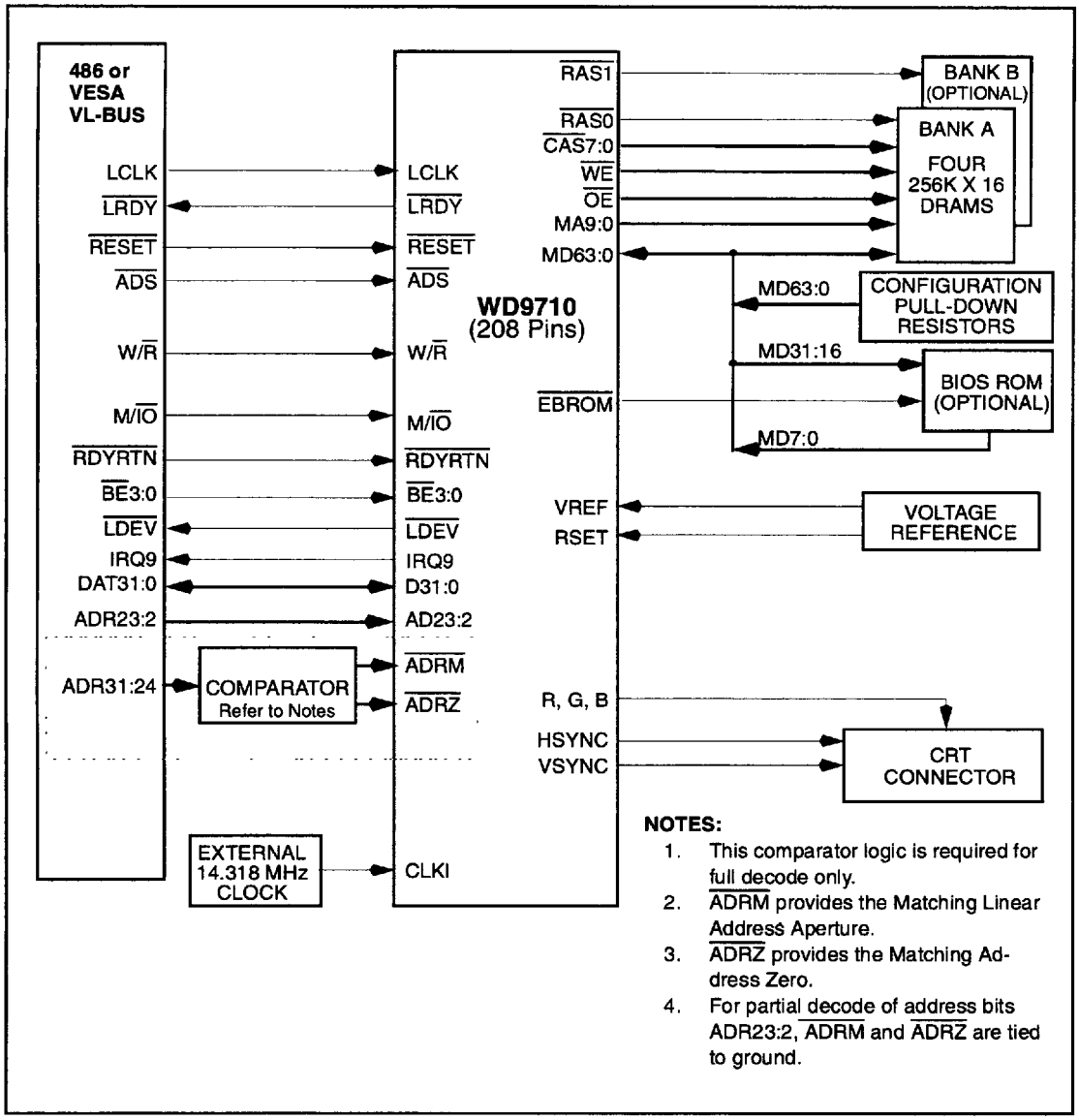


FIGURE 3-4. DE-MULTIPLEXED VL-BUS INTERFACE

3.6 MULTIPLEXED VESA VL-BUS WITH EXTERNAL RAMDAC INTERFACE (16-BIT)

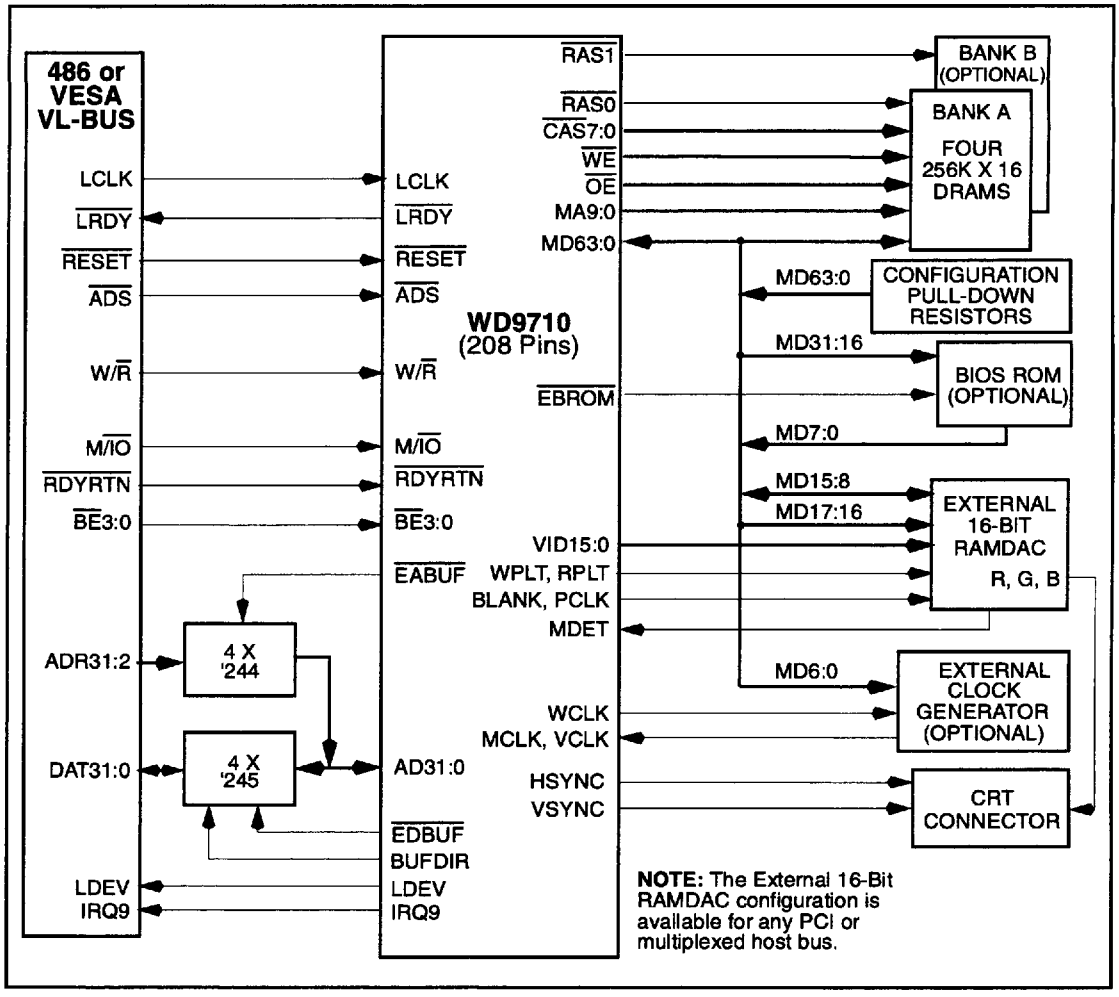


FIGURE 3-5. MULTIPLEXED VESA VL-BUS WITH EXTERNAL RAMDAC INTERFACE (16-BIT)

4.0 DISPLAY MEMORY CONFIGURATIONS

4.1 DISPLAY MEMORY OPERATION

The WD9710 operates with either a 32-bit or 64-bit display memory interface and accommodates one, two, or four megabytes of display memory. The display memory size required depends on the display resolution, color depth, and desired performance level.

The access time needed for display memory depends on the MCLK frequency. Table 4-1 lists the recommended frequencies for commonly available DRAM speeds. Some DRAMs may required higher or lower clock rates depending upon their operating parameters.

MCLK (MHz)	DRAM SPEED (ns)	DRAM SPEED WITH EDO (ns)
50	70	---
55	70	---
60	60	70
65	60	70
70	50	60
75	45	60
80	45	60

TABLE 4-1. REOMMENDED MEMORY ACCESS TIMES

4.2 GRAPHICS AND MOTION VIDEO DISPLAY MODES SUPPORTED

Table 4-2 lists the graphics display modes supported by the WD9710 while displaying a full motion YUV data window. The scaling and interpolation of the motion video window is limited in size only by the size of the graphics display mode. Although a configuration operates with only 1M byte of display memory, the same configuration may achieve much higher performance with 2M bytes or more of display memory.

RESOLUTION	COLOR DEPTH	MINIMUM MEMORY REQUIRED (MB)1	REFRESH RATES (Hz)					
			INTERLACED	60	70	72	75	75+2
640 x 480 x 8	256	1	---	A	A	B	B	B
640 x 480 x 16	65,536	1	---	B	C	C	C	C
800 x 600 x 8	256	1	---	C	C	C	C	C
800 x 600 x 16	65,536	2	---	A	B	B	B	B
1024 x 768 x 8	256	2	---	A	C	C	C	C
1024 x 768 x 16	65,536	2	---	C	C	C	C	C
1280 x 1024 x 8	256	2	B	---	---	---	---	---
1280 x 1024 x 16	65,536	4	B	---	---	---	---	---
1600 x 1200 x 8	256	2	C	---	---	---	---	---

NOTES:

(1) Although 1 megabyte (MB) is the minimum memory requirement, the same configuration may achieve a much higher performance with 2 MB or more of display memory.

(2) The 75+ Hz refresh rate refers to the greater than 75 Hz rates that are not yet defined by VESA.

(3) The letters in the refresh rate columns indicate conditions for listed resolution as follows:

A = No MCLK restrictions apply.

B = MCLK must be 60 MHz minimum.

C = MCLK must be 80 MHz minimum.

D = Requires a pixel clock faster than 135 MHz. An external RAMDAC is required.

TABLE 4-2. GRAPHICS AND MOTION VIDEO DISPLAY MODES SUPPORTED

4.3 GRAPHICS DISPLAY MODES SUPPORTED

Table 4-3 lists the graphics display modes supported by the WD9710. Although a configuration operates with only 1M byte of display memory, the same configuration may achieve much higher performance with 2M bytes or more of display memory.

RESOLUTION	COLOR DEPTH	MINIMUM MEMORY REQUIRED (MB)[1]	REFRESH RATES (Hz)					
			INTERLACED	60	70	72	75	75+[2]
640 x 480 x 4	16	1	---	A	A	A	A	A
640 x 480 x 8	256	1	---	A	A	A	A	A
640 x 480 x 16	65,536	1	---	A	A	A	A	A
640 x 480 x 24	16.8 MB	2	---	A	A	A	A	A
640 x 480 x 24 (packed mode)	16.8 MB	1	---	B	---	---	---	---
800 x 600 x 4	16	1	---	A	A	A	A	A
800 x 600 x 8	256	1	---	A	A	A	A	A
800 x 600 x 16	65,536	1	---	A	A	B	B	B
800 x 600 x 24	16.8 MB	2	---	A	A	B	B	B
1024 x 768 x 4	16	1	---	A	A	A	A	A
1024 x 768 x 8	256	1	---	A	A	A	A	A
1024 x 768 x 16	65,536	2	---	A	A	A	A	A
1024 x 768 x 24	16.8 MB	4	---	C	C	---	---	---
1280 x 1024 x 4	16	1	---	A	A	A	A	D
1280 x 1024 x 8	256	2	---	A	A	A	A	D
1280 x 1024 x 16	65,536	4	A	---	---	---	---	---
1600 x 1200 x 4	16	1	A	D	---	---	---	---
1600 x 1200 x 8	256	2	A	D	---	---	---	---

NOTES:

(1) Although 1 megabyte (MB) is the minimum memory requirement, the same configuration may achieve a much higher performance with 2 MB or more of display memory.

(2) The 75+ Hz refresh rate refers to the greater than 75 Hz rates that are not yet defined by VESA.

(3) The letters in the refresh rate columns indicate conditions for listed resolution as follows:

A = No MCLK restrictions apply.

B = MCLK must be 60 MHz minimum.

C = MCLK must be 80 MHz minimum.

D = Requires a pixel clock faster than 135 MHz. An external RAMDAC is required.

TABLE 4-3. GRAPHICS DISPLAY MODES SUPPORTED

5.0 SIGNAL DESCRIPTIONS

This section contains detailed information concerning signals and connector pins for the WD9710 controller 208-pin MQFP package. The following information is contained in this section:

- Multiplexed Signal to Pin Location Table
- Multiplexed Signal to Pin Location Diagram
- De-multiplexed Signal to Pin Location Table
- De-multiplexed Signal to Pin Location Diagram
- PCI Bus Signal to Pin Location Table
- PCI Bus Signal to Pin Location Diagram
- Detailed Signal Descriptions
- Display Memory Connections
- Multiplexed Host Bus Connections
- Host Interface Shared Pins
- Monitor/VAFC/Clock Connections
- Display Memory Bus Shared Connections
- External Component Connector Pins
- Miscellaneous Control Connections
- Power and Ground Connections

5.1 MULTIPLEXED SIGNAL NAME TO PIN LOCATION

Table 5-1 lists all of the WD9710 connector pins in ascending order with the signals given for the multiplexed host bus configuration (see Figure 5-1). Where two or more signals are listed for the same pin, the signal names are separated by a reverse virgule (\). To determine to application for a particular signal, refer to the signal descriptions in Table 5-4. Connections for the de-multiplexed host bus configuration are listed in Table 5-2. For PCI-bus connections refer to Table 5-3. For VAFC and RAMDAC connections refer to Table 5-9.

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - VSS	31 - MD39	61 - MD62	91 - AD10
2 - MD03\Q3\ EXTCLKSEL3	32 - $\overline{\text{CAS4}}$	62 - MD63	92 - VCC
3 - MD02\Q2\ EXTCLKSEL2	33 - VSS	63 - $\overline{\text{CAS7}}$	93 - AD11
4 - MD01\Q1\ EXTCLKSEL1	34 - MD40	64 - IRQ9\IRQ	94 - AD12
5 - MD00\Q0\ EXTCLKSEL0	35 - MD41	65 - $\overline{\text{RESET}}$	95 - AD13
6 - $\overline{\text{CAS0}}$	36 - MD42	66 - LCLK\EMEM	96 - VSS
7 - $\overline{\text{RAS0}}$	37 - MD43	67 - $\overline{\text{BE3}}$\AEN	97 - AD14
8 - MA9	38 - MD44	68 - $\overline{\text{BE2}}$\$\overline{\text{IOR}}$	98 - AD15
9 - MA8	39 - MD45	69 - $\overline{\text{ADS}}$\BALE	99 - AD16\SLA16
10 - MA7	40 - MD46	70 - $\overline{\text{RDYRTN}}$\$\overline{\text{IOW}}$	100 - AD17\SLA17
11 - MA6	41 - MD47	71 - $\overline{\text{LRDY}}$\IOCHRDY	101 - VCC
12 - VCC	42 - $\overline{\text{CAS5}}$	72 - VCC	102 - AD18\SLA18
13 - MA5	43 - VSS	73 - $\overline{\text{LDEV}}$\$\overline{\text{MEMCS16}}$	103 - VSS
14 - MA4	44 - MD48	74 - W/$\overline{\text{R}}$\$\overline{\text{IOCS16}}$	104 - AD19\SLA19
15 - $\overline{\text{WE}}$	45 - MD49	75 - $\overline{\text{BE1}}$\$\overline{\text{SBHE}}$	105 - AD20\SLA20
16 - VSS	46 - MD50	76 - $\overline{\text{BE0}}$\$\overline{\text{MEMW}}$	106 - AD21\SLA21
17 - MA3	47 - MD51	77 - VSS	107 - AD22\SLA22
18 - MA2	48 - VCC	78 - M/$\overline{\text{IO}}$\$\overline{\text{MEMR}}$	108 - AD23\SLA23
19 - MA1	49 - MD52	79 - D0\AD0	109 - VSS
20 - MA0	50 - MD53	80 - D1\AD1	110 - AD31
21 - $\overline{\text{OE}}$	51 - MD54	81 - AD2	111 - VCC
22 - $\overline{\text{RAS1}}$	52 - MD55	82 - AD3	112 - AD30
23 - MD32	53 - $\overline{\text{CAS6}}$	83 - VCC	113 - AD29
24 - MD33	54 - VSS	84 - AD4	114 - AD28
25 - MD34	55 - MD56	85 - AD5	115 - AD27
26 - MD35	56 - MD57	86 - VSS	116 - VSS
27 - VCC	57 - MD58	87 - AD6	117 - AD26
28 - MD36	58 - MD59	88 - AD7	118 - AD25
29 - MD37	59 - MD60	89 - AD8	119 - AD24
30 - MD38	60 - MD61	90 - AD9	120 - VCC

TABLE 5-1. MULTIPLEXED SIGNAL NAME TO PIN LOCATION

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
121 - $\overline{\text{EABUF}}$	143 - VID3	165 - USR1	187 - MD22\A6
122 - $\overline{\text{EDBUF}}$	144 - VID2	166 - USR0	188 - MD21\A5
123 - BUFDIR	145 - VID1	167 - VCC	189 - MD20\A4
124 - $\overline{\text{BLANK}}$	146 - VID0	168 - MCLK	190 - VSS
125 - $\overline{\text{RPLT}}$\MVCLK	147 - VSS	169 - MCAP	191 - MD19\A3
126 - $\overline{\text{WPLT}}$\GRDY	148 - RVSS	170 - CVCC	192 - MD18\A2
127 - $\overline{\text{EXVID}}$	149 - B (analog out)	171 - VCAP	193 - MD17\A1\RS1
128 - PCLK\DCLK	150 - DVSS	172 - CLKI\VCLK	194 - MD16\A0\RS0
129 - VSS	151 - RSET\MDET	173 - CVSS	195 - CAS1
130 - WCLK\VID15	152 - G (analog out)	174 - VSS	196 - MD15\D7
131 - $\overline{\text{EXPCLK}}$\VID14	153 - VREF (analog in)	175 - $\overline{\text{CAS3}}$	197 - MD14\D6
132 - $\overline{\text{EXSYNC}}$\VID13	154 - DVSS	176 - MD31\A15	198 - MD13\D5
133 - VID12	155 - R (analog out)	177 - MD30\A14	199 - MD12\D4
134 - VID11	156 DVCC	178 - MD29\A13	200 - MD11\D3
135 - VID10	157 RVCC	179 - MD28\A12	201 - MD10\D2
136 - VID9	158 USR4	180 - MD27\A11	202 - MD09\D1
137 - VID8\VIDS	159 USR3	181 - MD26\A10	203 - MD08\D0
138 - VCC	160 VSYNC	182 - MD25\A9	204 - VCC
139 - VID7	161 HSYNC	183 - MD24\A8	205 - MD07\Q7
140 - VID6	162 VSS	184 - $\overline{\text{CAS2}}$	206 - MD06\Q6
141 - VID5	163 $\overline{\text{EBROM}}$	185 - VCC	207 - MD05\Q5\ EXTCLKSEL5
142 - VID4	164 USR2	186 - MD23\A7	208 - MD04\Q4\ EXTCLKSEL4

TABLE 5-1. MULTIPLEXED SIGNAL NAME TO PIN LOCATION (Continued)

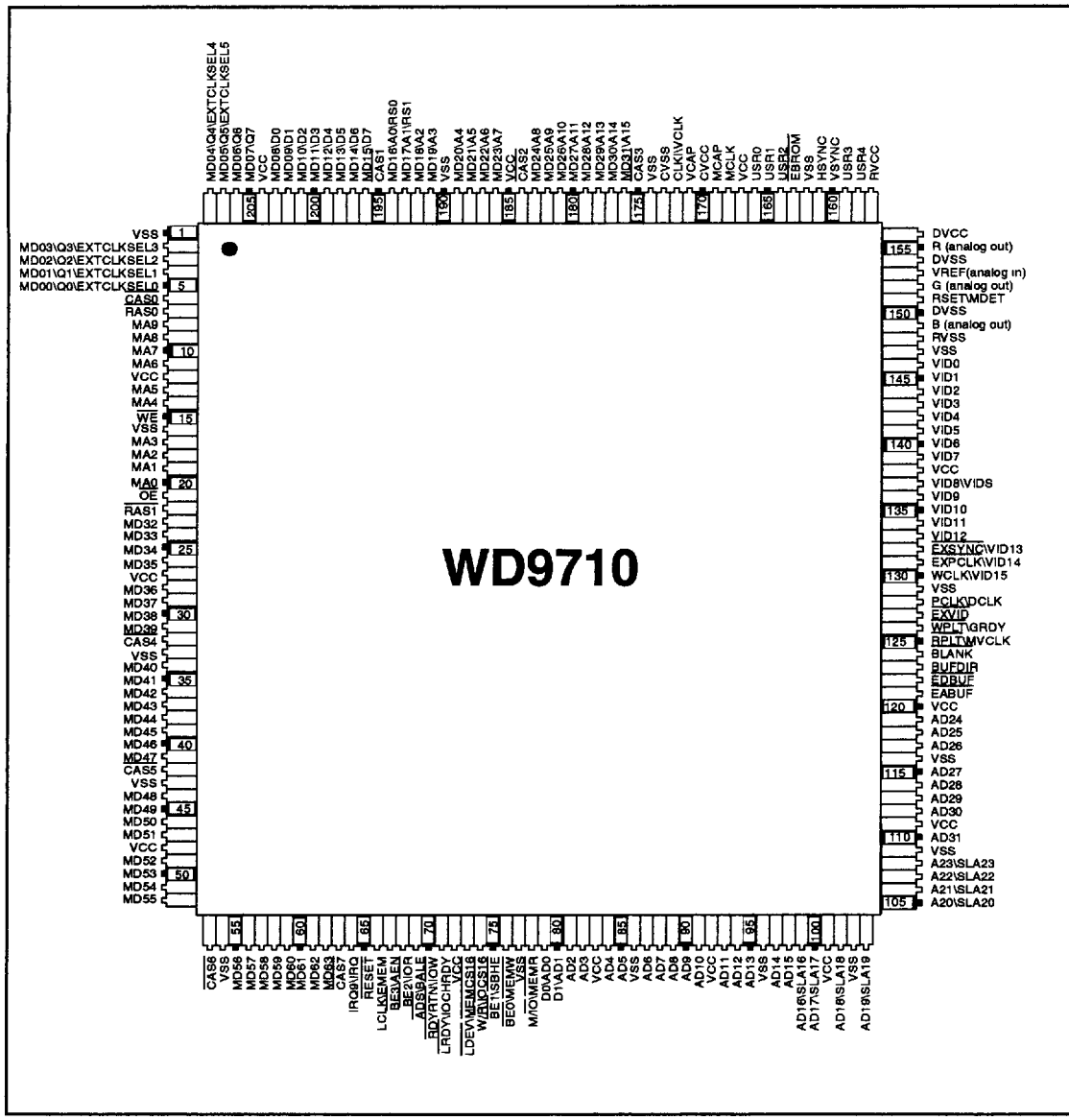


FIGURE 5-1. MULTIPLEXED SIGNAL NAME TO PIN LOCATIONS

5.2 DE-MULTIPLEXED SIGNAL NAME TO PIN LOCATION

Table 5-2 lists all of the WD9710 connector pins in ascending order with the signals names given for the de-multiplexed host bus configuration (see Figure 5-2).Where two or more signals are listed for the same pin, the signal names are separated by a reverse virgule (\). To determine to application for a particular signal, refer to the signal descriptions in Table 5-4. Connections for the multiplexed host bus configuration are listed in Table 5-1. For PCI-bus connections refer to Table 5-3. For VAFC and RAMDAC connections refer to Table 5-9.

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - VSS	31 - MD39	61 - MD62	91 - A10\SLA10
2 - MD03\Q3\ EXTCLKSEL3	32 - $\overline{\text{CAS4}}$	62 - MD63	92 - VCC
3 - MD02\Q2\ EXTCLKSEL2	33 - VSS	63 - $\overline{\text{CAS7}}$	93 - A11\SLA11
4 - MD01\Q1\ EXTCLKSEL1	34 - MD40	64 - IRQ9\IRQ	94 - A12\SLA12
5 - MD0\Q0\ EXTCLKSEL0	35 - MD41	65 - $\overline{\text{RESET}}$	95 - A13\SLA13
6 - $\overline{\text{CAS0}}$	36 - MD42	66 - LCLK\EMEM	96 - VSS
7 - $\overline{\text{RAS0}}$	37 - MD43	67 - $\overline{\text{BE3}}$\AEN	97 - A14\SLA14
8 - MA9	38 - MD44	68 - $\overline{\text{BE2}}$\$\overline{\text{IOR}}$	98 - A15\SLA15
9 - MA8	39 - MD45	69 - $\overline{\text{ADS}}$\BALE	99 - A16\SLA16
10 - MA7	40 - MD46	70 - $\overline{\text{RDYRTN}}$\$\overline{\text{IOW}}$	100 - A17\SLA17
11 - MA6	41 - MD47	71 - $\overline{\text{LRDY}}$\IOCHRDY	101 - VCC
12 - VCC	42 - $\overline{\text{CAS5}}$	72 - VCC	102 - A18\SLA18
13 - MA5	43 - VSS	73 - $\overline{\text{LDEV}}$\$\overline{\text{MEMCS16}}$	103 - VSS
14 - MA4	44 - MD48	74 - W/$\overline{\text{R}}$\$\overline{\text{IOCS16}}$	104 - A19\SLA19
15 - $\overline{\text{WE}}$	45 - MD49	75 - $\overline{\text{BE1}}$\$\overline{\text{SBHE}}$	105 - A20\SLA20
16 - VSS	46 - MD50	76 - $\overline{\text{BE0}}$\$\overline{\text{MEMW}}$	106 - A21\SLA21
17 - MA3	47 - MD51	77 - VSS	107 - A22\SLA22
18 - MA2	48 - VCC	78 - M/$\overline{\text{IO}}$\$\overline{\text{MEMR}}$	108 - A23\SLA23
19 - MA1	49 - MD52	79 - $\overline{\text{ADRZ}}$\SLA0	109 - VSS
20 - MA0	50 - MD53	80 - $\overline{\text{ADRM}}$\SLA1	110 - D31\$\overline{\text{SRDY}}$
21 - $\overline{\text{OE}}$	51 - MD54	81 - A2\SLA2	111 - VCC
22 - $\overline{\text{RAS1}}$	52 - MD55	82 - A3\SLA3	112 - D30
23 - MD32	53 - $\overline{\text{CAS6}}$	83 - VCC	113 - D29
24 - MD33	54 - VSS	84 - A4\SLA4	114 - D28
25 - MD34	55 - MD56	85 - A5\SLA5	115 - D27
26 - MD35	56 - MD57	86 - VSS	116 - VSS
27 - VCC	57 - MD58	87 - A6\SLA6	117 - D26
28 - MD36	58 - MD59	88 - A7\SLA7	118 - D25
29 - MD37	59 - MD60	89 - A8\SLA8	119 - D24
30 - MD38	60 - MD61	90 - A9\SLA9	120 - VCC

TABLE 5-2. DE-MULTIPLEXED SIGNAL NAME TO PIN LOCATION

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
121 - D23	143 - D3	165 - USR1	187 - MD22\A6
122 - D22	144 - D2	166 - USR0	188 - MD21\A5
123 - D21	145 - D1	167 - VCC	189 - MD20\A4
124 - D20	146 - D0	168 - MCLK	190 - VSS
125 - D19	147 - VSS	169 - MCAP	191 - MD19\A3
126 - D18	148 - RVSS	170 - CVCC	192 - MD18\A2
127 - D17	149 - B (analog out)	171 - VCAP	193 - MD17\A1\RS1
128 - D16	150 - DVSS	172 - CLKI\VCLK	194 - MD16\A0\RS0
129 - VSS	151 - RSET\MDET	173 - CVSS	195 - $\overline{\text{CAS1}}$
130 - D15	152 - G (analog out)	174 - VSS	196 - MD15\D7
131 - D14	153 - VREF (analog in)	175 - $\overline{\text{CAS3}}$	197 - MD14\D6
132 - D13	154 - DVSS	176 - MD31\A15	198 - MD13\D5
133 - D12	155 - R (analog out)	177 - MD30\A14	199 - MD12\D4
134 - D11	156 - DVCC	178 - MD29\A13	200 - MD11\D3
135 - D10	157 - RVCC	179 - MD28\A12	201 - MD10\D2
136 - D9	158 - USR4	180 - MD27\A11	202 - MD09\D1
137 - D8	159 - USR3	181 - MD26\A10	203 - MD8\D0
138 - VCC	160 - VSYNC	182 - MD25\A9	204 - VCC
139 - D7	161 - HSYNC	183 - MD24\A8	205 - MD07\Q7
140 - D6	162 - VSS	184 - $\overline{\text{CAS2}}$	206 - MD06\Q6
141 - D5	163 - $\overline{\text{EBROM}}$	185 - VCC	207 - MD5\Q5\ EXTCLKSEL5
142 - D4	164 - USR2	186 - MD23\A7	208 - MD4\Q4\ EXTCLKSEL4

TABLE 5-2. DE-MULTIPLEXED SIGNAL NAME TO PIN LOCATION (Continued)

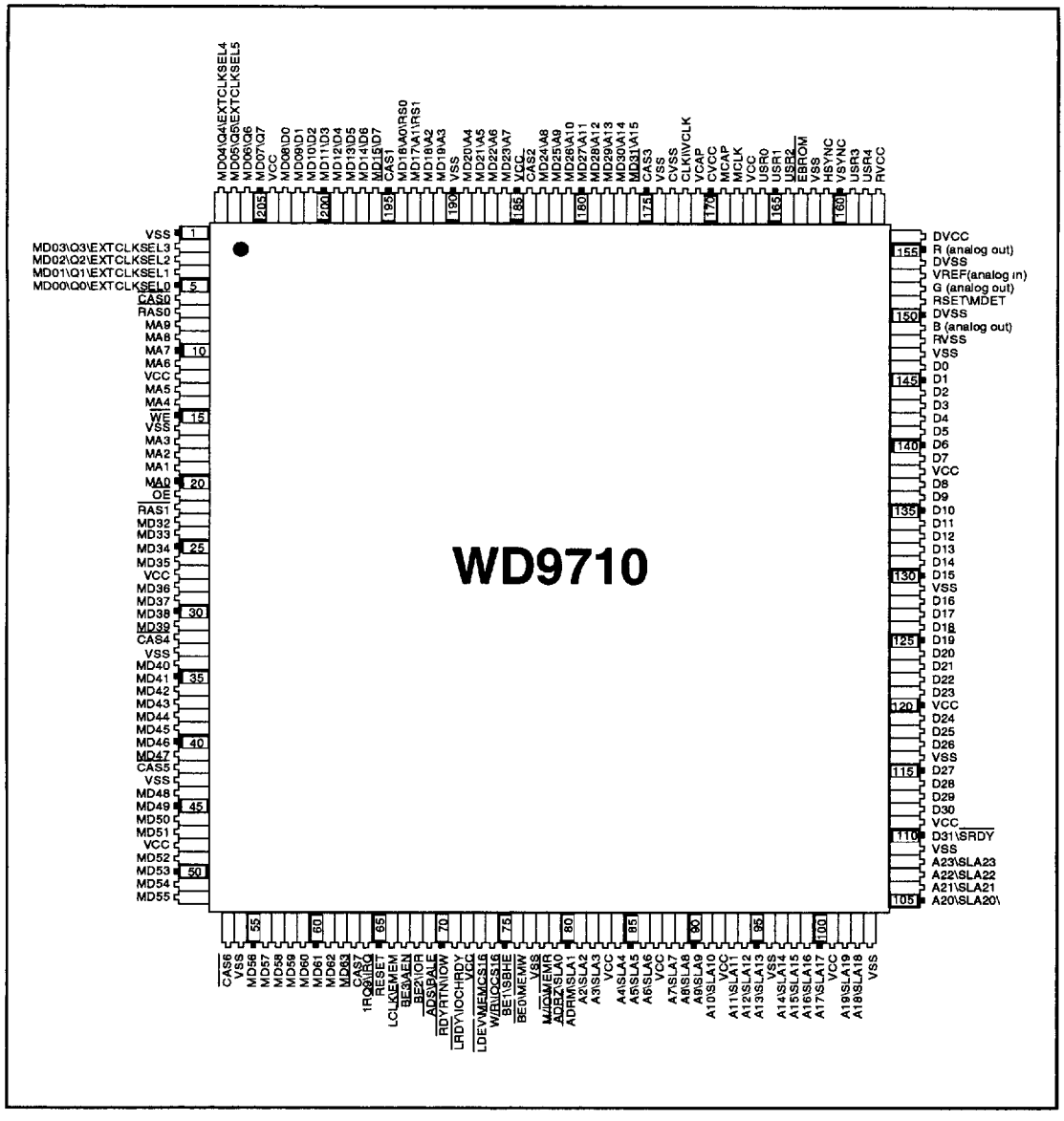


FIGURE 5-2. DE-MULTIPLEXED SIGNAL NAME TO PIN LOCATIONS

5.3 PCI BUS SIGNAL NAME TO PIN LOCATION

Table 5-3 lists all of the WD9710 connector pins in ascending order with the signals names given for the multiplexed PCI bus configuration (see Figure 5-3). Where two or more signals are listed for the same pin, the signal names are separated by a reverse virgule (\). To determine to application for a particular signal, refer to the signal descriptions in Table 5-4. Connections for the multiplexed host bus configuration are listed in Table 5-1. Connections for the de-multiplexed host bus configuration are listed in Table 5-2. For VAFC and RAMDAC connections refer to Table 5-9.

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - VSS	31 - MD39	61 - MD62	91 - AD10
2 - MD03\Q3\ EXTCLKSEL3	32 - $\overline{\text{CAS4}}$	62 - MD63	92 - VCC
3 - MD02\Q2\ EXTCLKSEL2	33 - VSS	63 - $\overline{\text{CAS7}}$	93 - AD11
4 - MD01\Q1\ EXTCLKSEL1	34 - MD40	64 - IRQ	94 - AD12
5 - MD00\Q0\ EXTCLKSEL0	35 - MD41	65 - $\overline{\text{RST}}$	95 - AD13
6 - $\overline{\text{CAS0}}$	36 - MD42	66 - CLK	96 - VSS
7 - $\overline{\text{RAS0}}$	37 - MD43	67 - C/$\overline{\text{BE3}}$	97 - AD14
8 - MA9	38 - MD44	68 - C/$\overline{\text{BE2}}$	98 - AD15
9 - MA8	39 - MD45	69 - $\overline{\text{FRAME}}$	99 - AD16
10 - MA7	40 - MD46	70 - $\overline{\text{IRDY}}$	100 - AD17
11 - MA6	41 - MD47	71 - $\overline{\text{TRDY}}$	101 - VCC
12 - VCC	42 - $\overline{\text{CAS5}}$	72 - VCC	102 - AD18
13 - MA5	43 - VSS	73 - $\overline{\text{DEVSEL}}$	103 - VSS
14 - MA4	44 - MD48	74 - $\overline{\text{STOP}}$	104 - AD19
15 - $\overline{\text{WE}}$	45 - MD49	75 - C/$\overline{\text{BE1}}$	105 - AD20
16 - VSS	46 - MD50	76 - C/$\overline{\text{BE0}}$	106 - AD21
17 - MA3	47 - MD51	77 - VSS	107 - AD22
18 - MA2	48 - VCC	78 - $\overline{\text{CHIPKILL}}$	108 - AD23
19 - MA1	49 - MD52	79 - AD0	109 - VSS
20 - MA0	50 - MD53	80 - AD1	110 - AD31
21 - $\overline{\text{OE}}$	51 - MD54	81 - AD2	111 - VCC
22 - $\overline{\text{RAS1}}$	52 - MD55	82 - AD3	112 - AD30
23 - MD32	53 - $\overline{\text{CAS6}}$	83 - VCC	113 - AD29
24 - MD33	54 - VSS	84 - AD4	114 - AD28
25 - MD34	55 - MD56	85 - AD5	115 - AD27
26 - MD35	56 - MD57	86 - VSS	116 - VSS
27 - VCC	57 - MD58	87 - AD6	117 - AD26
28 - MD36	58 - MD59	88 - AD7	118 - AD25
29 - MD37	59 - MD60	89 - AD8	119 - AD24
30 - MD38	60 - MD61	90 - AD9	120 - VCC

TABLE 5-3. PCI BUS SIGNAL NAME TO PIN LOCATION

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
121 - PAR	143 - VID3	165 - USR1	187 - MD22\A6
122 - IDSEL	144 - VID2	166 - USR0	188 - MD21\A5
123 - No Connection	145 - VID1	167 - VCC	189 - MD20\A4
124 - $\overline{\text{BLANK0}}$	146 - VID0	168 - MCLK	190 - VSS
125 - $\overline{\text{RPLT}}$\MVCLK	147 - VSS	169 - MCAP	191 - MD19\A3
126 - $\overline{\text{WPLT}}$\GRDY	148 - RVSS	170 - CVCC	192 - MD18\A2
127 - $\overline{\text{EXVID}}$	149 - B (analog out)	171 - VCAP	193 - MD17\A1\RS1
128 - PCLK/DCLK	150 - DVSS	172 - CLKI\VCLK	194 - MD16\A0\RS0
129 - VSS	151 - RSET\MDET	173 - CVSS	195 - $\overline{\text{CAS1}}$
130 - WCLK\VID15	152 - G (analog out)	174 - VSS	196 - MD15\D7
131 - $\overline{\text{EXPCLK}}$\VID14	153 - VREF (analog in)	175 - $\overline{\text{CAS3}}$	197 - MD14\D6
132 - $\overline{\text{EXSYNC}}$\VID13	154 - DVSS	176 - MD31\A15	198 - MD13\D5
133 - VID12	155 - R (analog out)	177 - MD30\A14	199 - MD12\D4
134 - VID11	156 - DVCC	178 - MD29\A13	200 - MD11\D3
135 - VID10	157 - RVCC	179 - MD28\A12	201 - MD10\D2
136 - VID9	158 - USR4	180 - MD27\A11	202 - MD09\D1
137 - VID8\VIDS	159 - USR3	181 - MD26\A10	203 - MD08\D0
138 - VCC	160 - VSYNC	182 - MD25\A9	204 - VCC
139 - VID7	161 - HSYNC	183 - MD24\A8	205 - MD07\Q7
140 - VID6	162 - VSS	184 - $\overline{\text{CAS2}}$	206 - MD06\Q6
141 - VID5	163 - $\overline{\text{EBROM}}$	185 - VCC	207 - MD05\Q5\ EXTCLKSEL5
142 - VID4	164 - USR2	186 - MD23\A7	208 - MD04\Q4\ EXTCLKSEL4

TABLE 5-3. PCI BUS SIGNAL NAME TO PIN LOCATION (Continued)

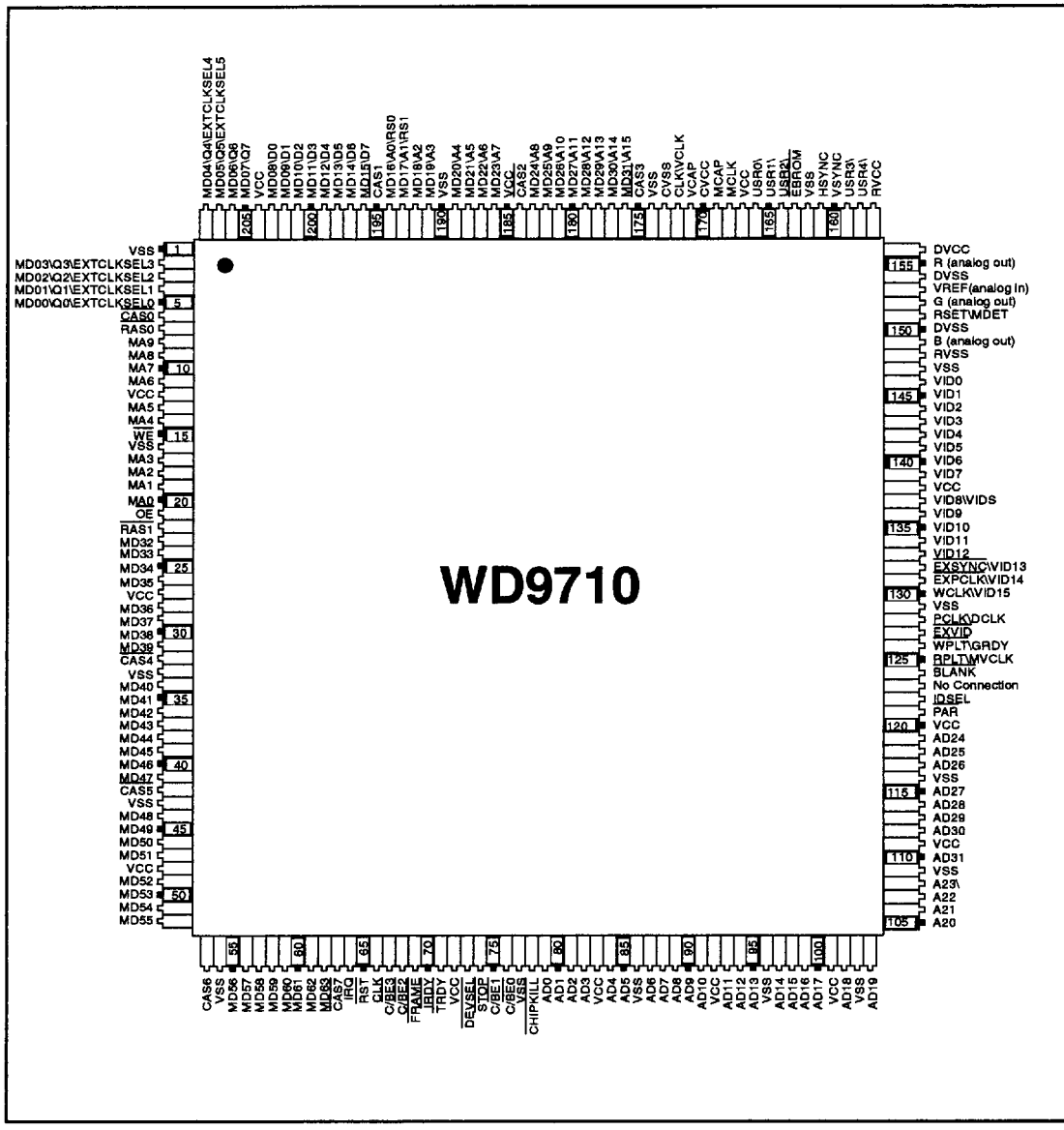


FIGURE 5-3. PCI BUS SIGNAL NAME TO PIN LOCATIONS

5.4 DETAILED SIGNAL DESCRIPTIONS

The following tables provide detailed descriptions of the signals connected to the WD9710 208-pin MQFP package. All of the signals are listed by their pin number and described in Table 5-4. Where more than one signal shares the same connector pin (multiplexed signals), each signal is described separately. Additional tables are provided to list signals in functional groups and to list signals that share the same connector pin (multiplexed) in functional groups. The following tables are provided in this section:

- Connector Pin Signal Definitions
- Display Memory Connections
- VESA VL-Bus Connections
- PCI-Bus Connections
- Host Interface Shared Pins
- Host Interface/VAFC Connector/RAMDAC Shared Pins
- Monitor/VAFC/Clock Connections
- Display Memory Bus Shared Pins
- External Device Connections
- Miscellaneous Control Connections
- Power and Ground Connections

5.5 SIGNAL DEFINITIONS

Table 5-4 lists the WD9710 input and output signal pins and the power and ground pins in the ascending pin number order without regard to the functional grouping of the signals. Functional groupings are provided in the subsequent tables. In addition to the pin number and signal name, Table 5-4 lists the bus interface associated with the signal, the signal type, and the signal description. In the BUS column, the bus interface is abbreviated as follows:

- PCI = PCI-Bus Connections
- MVL = Multiplexed VESA VL-Bus Connections
- DVL = De-multiplexed VESA VL-Bus Connections
- DMA = Display Memory Address Connections
- DMD = Display Memory Data Connections
- MRC = Monitor, RAMDAC, and Clock Connections
- PWR = Power and Ground Pins
- ROM = Read Only Memory
- VMC = VAFC Connector and Miscellaneous Control Pin Connections
- XCLK = External Clock Connections

In the TYPE column, Table 5-4 lists the active state of the signal as high, low, or tristate; and whether the signal is an input to or an output with regard to the WD9710.

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
1	VSS	PWR	---	**Ground** VSS = 0V
2 - 5	MD3:0	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 03 through 00** **Configuration Bits CNF3:0** Provide data bits 3 through 0 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF3 through CNF0 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
	Q3:0	ROM		**Read Only Memory Data Bits 3 through 0** Provide data bits 3 through 0 for Read Only Memory.
	EXTCLK SEL 3:0	XCLK		**External Clock Select Bits 3 through 0** Provide bits 3 through 0 for the 6-bit external clock select bus.
6	$\overline{CAS0}$	DMA	Active Low Output	**Column Address Strobe 0** Provides bit 0 of the 8-bit column address. Each line selects a column address for one DRAM. For duel $\overline{WE}$ configurations, $\overline{CAS}$7:1 are used as $\overline{WE}$7:1
7	$\overline{RAS0}$	DMA	Active Low Output	**Row Address Strobe 2** Selects the Row Address for DRAMs in memory bank 0.
8 - 11	MA9:6	DMA	Active High Output	**Memory Address Bus, Bits 9 through 6** Provides bits 9 through 6 of the 10-bit memory address to external display memory.
12	VCC	PWR	---	**Power** Main Power to Core Logic
13, 14	MA5, 4	DMA	Active High Output	**Memory Address Bus, Bits 5 and 4** Provides bits 5 and 4 of the 10-bit memory address to external display memory.
15	$\overline{WE}$	DMA	Active Low Output	**Write Enable Control** Provides write enable control for DRAMs.
16	VSS	PWR	---	**Ground** VSS = 0V
17 - 20	MA3:0	DMA	Active High Output	**Memory Address Bus, Bits 3 through 0** Provides bits 3 through 0 of the 10-bit memory address to external display memory.
21	$\overline{OE}$	DMA	Active Low Output	**Output Enable** Enables display memory output.
22	$\overline{RAS1}$	DMA	Active Low Output	**Row Address Strobe 1** Selects the Row Address for DRAMs in memory bank 1.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
23 - 26	MD32:35	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 32 through 35** **Configuration Bits CNF32:35** Provide data bits 32 through 35 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF32 through CNF35 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
27	VCC	PWR	---	**Power** Main Power to Core Logic
28- 31	MD36:39	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 36 through 39** **Configuration Bits CNF36:39** Provide data bits 36 through 39 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF36 through CNF39 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
32	$\overline{CAS}$4	DMA	Active Low Output	**Column Address Strobe 4** Provides bit 4 of the 8-bit column address. Each line selects a column address for one DRAM. For duel $\overline{WE}$ configurations, $\overline{CAS}$7:1 are used as $\overline{WE}$7:1
33	VSS	PWR	---	**Ground** VSS = 0V
34 - 41	MD40:47	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 40 through 47** **Configuration Bits CNF40:47** Provide data bits 40 through 47 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF40 through CNF47 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
42	$\overline{CAS}$5	DMA	Active Low Output	**Column Address Strobe 5** Provides bit 5 of the 8-bit column address. Each line selects a column address for one DRAM. For duel $\overline{WE}$ configurations, $\overline{CAS}$7:1 are used as $\overline{WE}$7:1
43	VSS	PWR	---	**Ground** VSS = 0V
44 - 47	MD48:51	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 48 through 51** **Configuration Bits CNF48:51** Provide data bits 48 through 51 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF48 through CNF51 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
48	VCC	PWR	---	**Power** Main Power to Core Logic
49-52	MD52:55	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 52 through 55** **Configuration Bits CNF52:55** Provide data bits 52 through 55 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF52 through CNF55 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
53	$\overline{CAS6}$	DMA	Active Low Output	**Column Address Strobe 6** Provides bit 6 of the 8-bit column address. Each line selects a column address for one DRAM. For duel $\overline{WE}$ configurations, $\overline{CAS}$7:1 are used as $\overline{WE}$7:1
54	VSS	PWR	---	**Ground** VSS = 0V
55 - 62	MD56:63	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 56 through 63** **Configuration Bits CNF56:63** Provide data bits 56 through 63 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF56 through CNF63 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
63	$\overline{CAS7}$	DMA	Active Low Output	**Column Address Strobe 7** Provides bit 7 of the 8-bit column address. Each line selects a column address for one DRAM. For duel $\overline{WE}$ configurations, $\overline{CAS}$7:1 are used as $\overline{WE}$7:1
64	IRQ9	MVL, DVL	Active High Output	**Interrupt Request 9** Programmable processor interrupt request for the VESA VL-Bus.
	IRQ	PCI		**Interrupt Request** Programmable processor interrupt request for the PCI Bus.
65	$\overline{RESET}$	MVL, DVL	Active Low Input	**System Reset** This signal resets the VESA VL-Local Bus Logic. Western Digital configuration bits are initialized at power-on and reset based on the logic level of the Display Buffer Memory bus as determined by pull up resistors.
	$\overline{RST}$	PCI		**System Reset** This signal resets the PCI Local Bus Logic. Western Digital configuration bits are initialized at power-on and reset based on the logic level of the Display Buffer Memory bus as determined by pull up resistors.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
66	LCLK	MVL, DVL	Active High Input	**CPU Clock** VL-Bus processor clock
	CLK	PCI		**PCI-Bus Clock** Processor Clock
67	$\overline{BE3}$	MVL, DVL	Active Low Input	**Byte Enable 3** Supports an enable for the VL-local bus low byte.
	C/$\overline{BE3}$	PCI		**Bus Command/Byte Enable 3** Supports an enable for the PCI-bus low byte.
68	$\overline{BE2}$	MVL, DVL	Active Low Input	**Byte Enable 2** Supports an enable for the VL-local bus next to low byte.
	C/$\overline{BE2}$	PCI		**Bus Command/Byte Enable 2** Supports an enable for the PCI-bus next to low byte.
69	$\overline{ADS}$	MVL, DVL	Active Low Input	**Address/Data Strobe** Supports the address and data strobe for transferring information over the VESA VL-Bus.
	$\overline{FRAME}$	PCI	Active Low Input	**Cycle Frame** Supports the cycle frame indicator for the PCI bus interface.
70	$\overline{RDYRTN}$	MVL DVL	Active Low Input	**Ready Return (From Host)** This signal is used for synchronizing the local bus with the host processor.
	$\overline{IRDY}$	PCI		**Initiator Ready** When active, this signal indicates that the device that initiated an access is ready to complete the current transaction.
71	$\overline{LRDY}$	MVL DVL	Active Low Output	**Local Bus Ready** Ready signal to host processor or Local Bus controller for the termination of the current instruction cycles.
	$\overline{TRDY}$	PCI		**Target Ready** When active, this signal indicates that the VGA is ready to complete the current transaction.
72	VCC	PWR	---	**Power** Main Power to Core Logic
73	$\overline{LDEV}$	MVL DVL	Active Low Output	**Local Bus Device Selected** Device selected on VL-bus.
	$\overline{DEVSEL}$	PCI	Active High Output	**Device Select** Device Selected on PCI-Bus

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
74	W/$\overline{R}$ (R=0)	MVL, DVL	Active Low Input	**Write or Read Cycle Status** Indicates the type of access occurring on the Local bus. When high, the access is a write operation, and when low the access is a read operation.
	$\overline{STOP}$ (0)	PCI	Active Low Input	**Stop** When active, this signal indicates that the VGA is requesting that the master stop a transaction.
75	$\overline{BE}$1	MVL, DVL	Active Low Input	**Byte Enable 1** Supports an enable for the VL-local bus next to high byte.
	C/$\overline{BE}$1	PCI		**Bus Command/Byte Enable 1** Supports an enable for the PCI-bus next to high byte.
76	$\overline{BE}$0	MVL, DVL	Active Low Input	**Byte Enable 0** Supports an enable for the VL-local bus high byte.
	C/$\overline{BE}$0	PCI		**Bus Command/Byte Enable 0** Provides an enable for the PCI-bus high byte.
77	VSS	PWR	---	**Ground** VSS = 0V
78	M/$\overline{IO}$	MVL, DVL	Active High/Low Input	**Memory or I/O Cycle Status** Local bus indicator for memory or I/O cycle. Low indicates an I/O cycle and high indicates a memory cycle.
	$\overline{CHIPKILL}$	PCI	Active Low Input	**Chip Kill** Allows host to turn off the WD9710 and allow another device to control the display.
79	D0	MVL	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bit 0** Provides bit 0 of the 32-bit multiplexed VL-bus host interface address and data.
	AD0	PCI		**PCI Host Interface Address/Data Bus Bit 0** Provides bit 0 of the 32-bit multiplexed PCI local bus host interface address and data.
	$\overline{ADRZ}$	DAV	Active Low Input	**Matching Address Zero** Output from an external comparator circuit that provides address bits ADR31:24 for full decode only. Tie ADRM and $\overline{ADRZ}$ to ground for partial decode of address bits ADR23:0.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
80	D1	MVL	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bit 01** Provides bit 1 of the 32-bit multiplexed VL-bus host interface address and data.
	AD1	PCI		**PCI Host Interface Address/Data Bus Bit 01** Provides bit 1 of the 32-bit multiplexed PCI local bus host interface address and data.
	$\overline{\text{ADRM}}$	DAV	Active Low Input	**Matching Linear Address Aperture** Output from an external comparator circuit that provides address bits ADR31:24 for full decode only. Tie $\overline{\text{ADRM}}$ and $\overline{\text{ADRZ}}$ to ground for partial decode of address bits ADR23:0.
81, 82	AD2, 3	MVL, PCI	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bits 2 and 3** • Provide bits 2 and 3 of the 32-bit multiplexed VL-bus local bus host interface address and data. • Provide bits 2 and 3 of the 32-bit multiplexed PCI local bus host interface address and data.
	A2, 3	DVL	Active High Input	**De-multiplexed VL-Bus Address Bits 2 and 3** Provide bits 2 and 3 of the 32-bit de-multiplexed VL-bus local bus host interface address and data.
83	VCC	PWR	---	**Power** Main Power to Core Logic
84, 85	AD4, 5	MVL, PCI	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bits 4 and 5** • Provide bits 4 and 5 of the 32-bit multiplexed VL-bus local bus host interface address and data. • Provide bits 4 and 5 of the 32-bit multiplexed PCI local bus host interface address and data.
	A4, 5	DVL	Active High Input	**De-multiplexed VL-Bus Address Bits 4 and 5** Provide bits 4 and 5 of the 32-bit de-multiplexed VL-bus local bus host interface address.
86	VSS	PWR	---	**Ground** VSS = 0V
87-91	AD6:10	MVL, PCI	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bits 6:10** • Provide bits 6 through 10 of the 32-bit multiplexed VL-bus local bus host interface address and data. • Provide bits 6 through 10 of the 32-bit multiplexed PCI local bus host interface address and data.
	A6:10	DVL	Active High Input	**De-multiplexed VL-Bus Address/Data Bits 6:10** Provide bits 6 through 10 of the 32-bit de-multiplexed VL-bus local bus host interface address.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
92	VCC	PWR	---	**Power** Main Power to Core Logic
93-95	AD11:13	MVL, PCI	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bits 11:13** • Provide bits 11 through 13 of the 32-bit multiplexed VL-bus local bus host interface address and data. • Provide bits 11 through 13 of the 32-bit multiplexed PCI local bus host interface address and data.
	A11:13	DVL	Active High Input	**De-multiplexed VL-Bus Address/Data Bits 11:13** Provide bits 11 through 13 of the 32-bit de-multiplexed VL-bus local bus host interface address.
96	VSS	PWR	---	**Ground** VSS = 0V
97-100	AD14:17	MVL, PCI	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bits 14:17** • Provide bits 14 through 17 of the 32-bit multiplexed VL-bus local bus host interface address and data. • Provide bits 14 through 17 of the 32-bit multiplexed PCI local bus host interface address and data.
	A14:17	DVL	Active High Input	**De-multiplexed VL-Bus Address/Data Bits 14:17** Provide bits 14 through 17 of the 32-bit de-multiplexed VL-bus local bus host interface address.
101	VCC	PWR	---	**Power** Main Power to Core Logic
102	AD18	MVL, PCI	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bit 18** • Provides bit 18 of the 32-bit multiplexed VL-bus local bus host interface address and data. • Provides bit 18 of the 32-bit multiplexed PCI local bus host interface address and data.
	A18	DVL	Active High Input	**De-multiplexed VL-Bus Address/Data Bit 18** Provides bit 18 of the 32-bit de-multiplexed VL-bus local bus host interface address.
103	VSS	PWR	---	**Ground** VSS = 0V

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
104-108	AD19:23	MVL, PCI	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bits 19:23** • Provide bits 19 through 23 of the 32-bit multiplexed VL-bus local bus host interface address and data. • Provide bits 19 through 23 of the 32-bit multiplexed PCI local bus host interface address and data.
	A19:23	DVL	Active High Input	**De-multiplexed VL-Bus Address/Data Bits 19:23** Provide bits 19 through 23 of the 32-bit de-multiplexed VL-bus local bus host interface address.
109	VSS	PWR	---	**Ground** VSS = 0V
110	AD31	MVL, PCI	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bit 31** • Provides bit 31 of the 32-bit multiplexed VL-bus host interface address and data. • Provides bit 31 of the 32-bit multiplexed PCI local bus host interface address and data.
	D31	DVL		**De-Multiplexed Host Interface Data Bus Bit 31** Provides bit 31 of the 32-bit de-multiplexed VL-bus host interface data bus.
111	VCC	PWR	---	**Power** Main Power to Core Logic
112-115	AD30:27	MVL, PCI	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bits 30:27** • Provides bits 30 through 27 of the 32-bit multiplexed VL-bus host interface address and data. • Provides bits 30 through 27 of the 32-bit multiplexed PCI local bus host interface address and data.
	D30:D27	DVL		**De-Multiplexed Host Interface Data Bus Bits 30:27** Provide bits 30 through 24 of the 32-bit de-multiplexed VL-bus host interface data bus.
116	VSS	PWR	---	**Ground** VSS = 0V
117-119	AD26:24	MVL, PCI	Active High Input/Output	**Multiplexed Host Interface Address/Data Bus Bits 26:24** • Provides bits 26 through 24 of the 32-bit multiplexed VL-bus host interface address and data. • Provides bits 26 through 24 of the 32-bit multiplexed PCI local bus host interface address and data.
	D27:D24	DVL		**De-Multiplexed Host Interface Data Bus Bits 26:24** Provide bits 26 through 24 of the 32-bit de-multiplexed VL-bus host interface data bus.
120	VCC	PWR	---	**Power** Main Power to Core Logic

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
121	$\overline{\text{EABUF}}$	MVL	Active Low Output	**Enable Address Buffer** Used to control the address and data multiplexers.
	PAR	PCI	Active High Output	**Parity** This signal supports even parity across the PCI address/ data bus (AD31:0)
	D23	DVL	Active High Input/Output	**De-multiplexed VESA VL-Bus Data Bit 23** Provides bit 23 of the 24-bit de-multiplexed VL-bus host interface data.
122	$\overline{\text{EDBUF}}$	MVL	Active Low Output	**Enable Data Buffer** Used to control the address and data multiplexers.
	IDSEL	PCI	Active High Input	**Initialization Device Select** PCI-bus initialization control.
	D22	DVL	Active High Input/Output	**De-multiplexed VESA VL-Bus Data Bit 22** Provides bit 22 of the 24-bit de-multiplexed VL-bus host interface data.
123	BUFDIR	MVL	Active High Output	**Data Buffer Direction** Used to control the address and data multiplexers.
	D21	DVL	Active High Input/Output	**De-multiplexed VESA VL-Bus Data Bit 21** Provides bit 21 of the 24-bit de-multiplexed VL-bus host interface data.
124	$\overline{\text{BLANK}}$	MRC	Active Low Input/Output	**RAMDAC Blanking Control** This signal provides the standard analog VGA RAMDAC blanking signal.
	$\overline{\text{BLANK}}$	VMC	Active Low Output	**VAFC Blanking Control** Provides screen blanking signal on pin 9 for VAFC operation
	D20	DVL		**De-multiplexed VESA VL-Bus Data Bit 20** Provides bit 20 of the 24-bit de-multiplexed VL-bus host interface data.
125	$\overline{\text{RPLT}}$	MRC	Active Low Output	**Read Palette** This signal is the read pulse to an external RAMDAC or equivalent circuit.
	MVCLK	VMC	Active High Input	**VAFC VCLK Clock** Provides video clock (VCLK) on pin 13 for VAFC connector.
	D19	DVL	Active High Input/Output	**De-multiplexed VESA VL-Bus Data Bit 19** Provides bit 19 of the 24-bit de-multiplexed VL-bus host interface data.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
126	$\overline{\text{WPLT}}$	MRC	Active Low Output	**Write Palette** This signal is the write pulse to an external RAMDAC or equivalent circuit.
	GRDY	VMC	Active High Output	**VAFC Graphics Ready** Provides Graphics Ready signal on pin 8 of the VAFC connector.
	D18	DVL	Active High Input/Output	**De-multiplexed VESA VL-Bus Data Bit 18** Provides bit 18 of the 24-bit de-multiplexed VL-bus host interface data.
127	$\overline{\text{EXVID}}$	VMC	Active Low Input	**VAFC Video Enable** Provides video enable signal on pin 16 of the VAFC connector.
	D17	DVL	Active High Input/Output	**De-multiplexed VESA VL-Bus Data Bit 17** Provides bit 17 of the 24-bit de-multiplexed VL-bus host interface data.
128	PCLK	MRC	Active High Output	**Pixel Clock** Video pixel clock output used by the external RAMDAC to latch pixel data from the WD9710 controller's video output bus into an external RAMDAC or equivalent circuit. Pixel data changes on the rising edge of PCLK and is intended to be latched into an external RAMDAC or equivalent circuit by the falling edge of PCLK.
	DCLK	VMC	Active High Output	**VAFC Master Clock** Provides the master clock signal on pin 15 of the VAFC connector.
	D16	DVL		**De-multiplexed VESA VL-Bus Data Bit 16** Provides bit 16 of the 24-bit de-multiplexed VL-bus host interface data.
129	VSS	PWR	---	**Ground** VSS = 0V
130	WCLK	MRC	Active High Output	**Clock Generator Write Strobe** Enables programming of clock generator frequency.
	VID15	MRC		**Video Output To Palette, Bit 15** Provides bit 15 of the 16-bit multiplexed host bus video output.
	VID15	VMC	Active High Input	**VAFC Data Input, Bit 15** Provides bit 15 of the 16-bit data input on pin 28 of the VAFC connector.
	D15	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 15** Provides bit 15 of the 24-bit de-multiplexed VL-bus host interface data.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
131	$\overline{\text{EXPCLK}}$	VMC	Active Low Output	**VMAC Connector Pixel Clock Enable** Provides the pixel clock output to the feature connector.
	VID14	MRC	Active High Output	**Video Output To Palette, Bit 14** Provides bit 14 of the 16-bit multiplexed host bus video output.
	VID14	VMC	Active High Input/	**VAFC Data Input, Bit 14** Provides bit 14 of the 16-bit data input on pin 67 of the VAFC connector.
	D14	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 14** Provides bit 14 of the 24-bit de-multiplexed VL-bus host interface data.
132	$\overline{\text{EXSYNC}}$	VMC	Active Low Output	**VMAC Connector Sync Enable** Provides the external sync pulse to the feature connector.
	VID13	MRC	Active High Output	**Video Output To Palette, Bit 13** Provides bit 13 of the 16-bit multiplexed host bus video output.
	VID13	VMC	Active High Input/	**VAFC Data Input, Bit 13** Provides bit 13 of the 16-bit data input on pin 66 of the VAFC connector.
	D13	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 13** Provides bit 13 of the 24-bit de-multiplexed VL-bus host interface data.
133	VID12	MRC	Active High Output	**Video Output To Palette, Bit 12** Provides bit 12 of the 16-bit multiplexed host bus video output.
	VID12	VMC	Active High Input/	**VAFC Data Input, Bit 12** Provides bit 12 of the 16-bit data input on pin 26 of the VAFC connector.
	D12	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 12** Provides bit 12 of the 24-bit de-multiplexed VL-bus host interface data.
134	VID11	MRC	Active High Output	**Video Output To Palette, Bit 11** Provides bit 11 of the 16-bit multiplexed host bus video output.
	VID11	VMC	Active High Input/	**VAFC Data Input, Bit 11** Provides bit 11 of the 16-bit data input on pin 25 of the VAFC connector.
	D11	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 11** Provides bit 11 of the 24-bit de-multiplexed VL-bus host interface data.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
135	VID10	MRC	Active High Output	**Video Output To Palette, Bit 10** Provides bit 10 of the 16-bit multiplexed host bus video output.
	VID10	VMC	Active High Input/	**VAFC Data Input, Bit 10** Provides bit 10 of the 16-bit data input on pin 64 of the VAFC connector.
	D10	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 10** Provides bit 10 of the 24-bit de-multiplexed VL-bus host interface data.
136	VID9	MRC	Active High Output	**Video Output To Palette, Bit 9** Provides bit 9 of the 16-bit multiplexed host bus video output.
	VID9	VMC	Active High Input/	**VAFC Data Input, Bit 9** Provides bit 9 of the 16-bit data input on pin 63 of the VAFC connector.
	D9	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 9** Provides bit 9 of the 24-bit de-multiplexed VL-bus host interface data.
137	VID8	MRC	Active High Output	**Video Output To Palette, Bit 8** Provides bit 8 of the 16-bit multiplexed host bus video output.
	VID8	MRC	Active High Input/	**VAFC Data Input, Bit 8** Provides bit 8 of the 16-bit data input on pin 23 of the VAFC connector.
	VIDS	VMC	Active High Output	**Video Output to Palette, 8-bit Select** Selects 8-bit video output mode.
	D8	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 8** Provides bit 8 of the 24-bit de-multiplexed VL-bus host interface data.
138	VCC	PWR	---	**Power** Main Power to Core Logic
139	VID7	MRC	Active High Output	**Video Output To Palette, Bit 7** Provides bit 7 of the 8-bit or 16-bit multiplexed host bus video output.
	VID7	VMC	Active High Input/	**VAFC Data Input, Bit 7** Provides bit 7 of the 16-bit data input on pin 22 of the VAFC connector.
	D7	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 7** Provides bit 7 of the 24-bit de-multiplexed VL-bus host interface data.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
140	VID6	MRC	Active High Output	**Video Output To Palette, Bit 6** Provides bit 6 of the 8-bit or 16-bit multiplexed host bus video output.
	VID6	VMC	Active High Input/	**VAFC Data Input, Bit 6** Provides bit 6 of the 16-bit data input on pin 61 of the VAFC connector.
	D6	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 6** Provides bit 6 of the 24-bit de-multiplexed VL-bus host interface data.
141	VID5	MRC	Active High Output	**Video Output To Palette, Bit 5** Provides bit 5 of the 8-bit or 16-bit multiplexed host bus video output.
	VID5	VMC	Active High Input/	**VAFC Data Input, Bit 5** Provides bit 5 of the 16-bit data input on pin 60 of the VAFC connector.
	D5	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 5** Provides bit 5 of the 24-bit de-multiplexed VL-bus host interface data.
142	VID4	MRC	Active High Output	**Video Output To Palette, Bit 4** Provides bit 4 of the 8-bit or 16-bit multiplexed host bus video output.
	VID4	VMC	Active High Input/	**VAFC Data Input, Bit 4** Provides bit 4 of the 16-bit data input on pin 20 of the VAFC connector.
	D4	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 4** Provides bit 4 of the 24-bit de-multiplexed VL-bus host interface data.
143	VID3	MRC	Active High Output	**Video Output To Palette, Bit 3** Provides bit 3 of the 8-bit or 16-bit multiplexed host bus video output.
	VID3	VMC	Active High Input/	**VAFC Data Input, Bit 3** Provides bit 3 of the 16-bit data input on pin 19 of the VAFC connector.
	D3	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 3** Provides bit 3 of the 24-bit de-multiplexed VL-bus host interface data.
144	VID2	MRC	Active High Output	**Video Output To Palette, Bit 2** Provides bit 2 of the 8-bit or 16-bit multiplexed host bus video output.
	VID2	VMC	Active High Input/	**VAFC Data Input, Bit 2** Provides bit 2 of the 16-bit data input on pin 58 of the VAFC connector.
	D2	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 2** Provides bit 2 of the 24-bit de-multiplexed VL-bus host interface data.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
145	VID1	MRC	Active High Output	**Video Output To Palette, Bit 1** Provides bit 1 of the 8-bit or 16-bit multiplexed host bus video output.
	VID1	VMC	Active High Input/	**VAFC Data Input, Bit 1** Provides bit 1 of the 16-bit data input on pin 57 of the VAFC connector.
	D1	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 1** Provides bit 1 of the 24-bit de-multiplexed VL-bus host interface data.
146	VID0	MRC	Active High Output	**Video Output To Palette, Bit 0** Provides bit 0 of the 8 bit or 16-bit multiplexed host bus video output.
	VID0	VMC	Active High Input/	**VAFC Data Input, Bit 0** Provides bit 0 of the 16-bit data input on pin 17 of the VAFC connector.
	D0	DVL	Active High Input/Output	**De-multiplexed System Data Bus Bit 0** Provides bit 0 of the 24-bit de-multiplexed VL-bus host interface data.
147	VSS	PWR	---	**Ground** VSS = 0V
148	RVSS	PWR	---	**Ground** Internal RAM Power Ground
149	B	MRC	Analog Output	**Internal RAMDAC Blue Output** High impedance current source that can directly drive a double-terminated 75-Ohm coaxial cable.
150	DVSS	PWR	---	**Ground** Internal DAC Power Ground
151	RSET/MDET	MRC	Analog Input	**Internal RAMDAC Full-Scale Control/ External RAMDAC Monitor Detect** RSET is used to set the full scale output current of the RED, GREEN, and BLUE DACs. MDET is used to detect the presence of a monitor.
152	G	MRC	Analog Output	**Internal RAMDAC Green Output** High impedance current source that can directly drive a double-terminated 75-Ohm coaxial cable.
153	VREF	MRC	Analog Input	**Internal RAMDAC Voltage Reference** An external voltage reference of 1.2V is connected to this input for normal operation of the internal RAMDAC.
154	DVSS	PWR	---	**Ground** Internal DAC Power Ground.
155	R	MRC	Analog Output	**Internal RAMDAC Red Output** High impedance current source that can directly drive a double-terminated 75-Ohm coaxial cable.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
156	DVCC	PWR	---	**Power** Power to Internal DAC.
157	RVCC	PWR	---	**Power** Power to Internal RAM.
158	USR4	DMT, MVL, DVL	Active High Output	**User Programmable Output Bit 4** This line, along with USR3:0 can be programmed by the user to initiate or confirm an WD9710 operation.
159	USR3	DMT, MVL, DVL	Active High Output	**User Programmable Output Bit 3** This line, along with USR4 and USR2:0 can be programmed by the user to initiate or confirm an WD9710 operation.
160	VSYNC	MRC	Active High Output	**Vertical Sync** VSYNC is the CRT vertical sync control signal output. It may be attached directly to the CRT monitor connections. Its active low or high level is programmable.
	VSYNC	VMC		**VAFC Vertical Sync** Provides the vertical sync signal to pin 10 of the VAFC connector.
161	HSYNC	MRC	Active High Output	**Horizontal Sync** HSYNC is the CRT horizontal sync control signal output. It may be attached directly to the CRT monitor connections. Its active low or high level is programmable as is its position and duration.
	HSYNC	VMC		**VAFC Horizontal Sync** Provides the horizontal sync signal to pin 10 of the VAFC connector.
162	VSS	PWR	---	**Ground** VSS = 0V
163	$\overline{\text{EBROM}}$	ROM, VMC	Active Low Output	**Enable BIOS ROM** This is an active low signal used to enable BIOS ROM (C0000h - C7FFFh).
164	USR2	DMT, MVL, DVL	Active High Output	**User Programmable Output Bit 2** This line, along with USR4, 3, 1, and 0 can be programmed by the user to initiate or confirm an WD9710 operation.
165	USR1	DMT, MVL, DVL	Active High Output	**User Programmable Output Bit 1** This line, along with USR4:2 and 0 can be programmed by the user to initiate or confirm an WD9710 operation.
166	USR0	DMT, MVL, DVL	Active High Output	**User Programmable Output Bit 0** This line, along with USR4:1 can be programmed by the user to initiate or confirm an WD9710 operation.
167	VCC	PWR	---	**Power** Main Power to Core Logic
168	MCLK	MRC	Active High Input	**Master Clock** Provides the master clock at programmable rates.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
169	MCAP	MRC	Active High Input	**Master Clock Analog Input** Connects to an external discrete filter network.
170	CVCC	PWR	---	**Power** Main Power to internal clock
171	VCAP	MVL, DVL	Active High Input	**Video Clock Analog Input** Connects to an external discrete filter network.
172	CLKI	MRC	Active High Input	**System Clock Input** Provides the CPU clock input (14.318 MHz).
	VCLK	MRC		**Video Clock** Provides the video shift clock at programmable rates.
173	CVSS	PWR	---	**Ground** Internal clock power ground
174	VSS	PWR	---	**Ground** VSS = 0V
175	$\overline{CAS3}$	DMA	Active Low Output	**Column Address Strobe 3** Provides bit 3 of the 8-bit column address. Each line selects a column address for one DRAM. For duel $\overline{WE}$ configurations, $\overline{CAS}$7:1 are used as $\overline{WE}$7:1
176, 177	MD31, 30	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 31 and 30** **Configuration Bits CNF31 and 30** Provide data bits 31 and 30 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF31 and CNF30 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
	A15, A14	ROM		**ROM Address** Provides bits 15 and 14 of the 16-bit ROM address.
	RS1, RS0	MRC		**RAMDAC Row Select** Selects RAMDAC row address. If RS2 is also present, it should be grounded.
178, 179	MD29, 28	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 29 and 28** **Configuration Bits CNF29 and 28** Provide data bits 29 and 28 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF29 and CNF28 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
	A13, A12	ROM		**ROM Address** Provides bits 13 and 12 of the 16-bit ROM address.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
180-183	MD27:24	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 27 through 24** **Configuration Bits CNF27 through 24.** Provide data bits 27 through 24 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF27 through CNF24 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
	A11:8	ROM		**ROM Address** Provides bits 11 through 8 of the 16-bit ROM address.
184	$\overline{CAS2}$	DMA	Active Low Output	**Column Address Strobe 2** Provides bit 2 of the 8-bit column address. Each line selects a column address for one DRAM. For duel $\overline{WE}$ configurations, $\overline{CAS}$7:1 are used as $\overline{WE}$7:1
185	VCC	PWR	---	**Power** Main Power to Core Logic
186-189	MD23:20	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 23 through 20** **Configuration Bits CNF23 through 20.** Provide data bits 23 through 20 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF23 through CNF20 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
	A7:4	ROM		**ROM Address** Provides bits 7 through 4 of the 16-bit ROM address.
190	VSS	PWR	---	**Ground** VSS = 0V
191-194	MD19:16	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 19 through 16** **Configuration Bits CNF19 through 16.** Provide data bits 19 through 16 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF19 through CNF16 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
	A3:0	ROM		**ROM Address** Provides bits 3 through 0 of the 16-bit ROM address.
195	$\overline{CAS1}$	DMA	Active Low Output	**Column Address Strobe 1** Provides bit 1 of the 8-bit column address. Each line selects a column address for one DRAM. For duel $\overline{WE}$ configurations, $\overline{CAS}$7:1 are used as $\overline{WE}$7:1

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

PIN NO.	SIGNAL NAME	BUS	TYPE	DESCRIPTION
196-203	MD15:08	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 15 through 8** **Configuration Bits CNF15 through 8.** Provide data bits 15 through 8 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF15 through CNF8 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
	D7:0	MRC		**Internal RAMDAC Data Bus** Provides bits 7 through 0 of the 8-bit Internal RAMDAC data.
204	VCC	PWR	---	**Power** Main Power to Core Logic
205	MD07	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bit 07** **Configuration Bit CNF7** Provides data bit 7 of the 64-bit memory data bus. During system turn on and reset, this pin provides configuration bit CNF7 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
	Q7	ROM		**Read Only Memory Data Bit 7** Provides data bit 7 for Read Only Memory. Bits D6 through D0 are located at pins 1 through 3 and 5 through 8, respectively.
206	MD06	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bit 06** **Configuration Bit CNF6** Provides data bit 6 of the 64-bit memory data bus. During system turn on and reset, this pin provides configuration bit CNF6 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
	Q6	ROM		**Read Only Memory Data Bit 6** Provides data bit 6 for Read Only Memory.
207, 208	MD5:4	DMD	Active High CMOS Input/Output Tristate w/ pull up	**Memory Data Bits 05 and 04** **Configuration Bits CNF5:4** Provide data bits 5 and 4 of the 64-bit memory data bus. During system turn on and reset, these pins provide configuration bits CNF5 and CNF4 of the 64-bit configuration register. The configuration bits are defined in subsequent sections.
	Q5:4	ROM		**Read Only Memory Data Bits 5 and 4** Provide data bits 5 and 4 for Read Only Memory.
	EXTCLK SEL5:4	XCLK		**External Clock Select Bits 5 and 4** Provide bits 5 and 4 for the 6-bit external clock select bus.

TABLE 5-4. WD9710 CONNECTOR PIN SIGNAL DEFINITIONS (Continued)

5.6 DISPLAY MEMORY CONNECTIONS

The following pins provide the display memory connections to the WD9710. These connections support conventional DRAMs.

PIN NO.	SIGNAL NAME	I/O	DESCRIPTION
8-11, 13, 14, 17-20	MA9:0	O	Memory Address
22, 7	$\overline{RAS}$1:0(1)	O	Memory Row Address Strobes
63, 53, 42, 32, 175, 184, 195, 6	$\overline{CAS}$7:0(1,2)	O	Memory Column Address Strobes
15	$\overline{WE}$	O	Memory Write Enable
21	$\overline{OE}$	O	Memory Output Enable
62-55, 52-49, 47-44, 41-34, 31-28, 26-23, 176-183, 186-189, 191-194, 196-203, 205-208,	MD63:0	I/O	Memory Data

NOTES:

(1) Configurations that do not require two pins for RAS or CAS drive both to permit load sharing.

(2) For dual-WE configurations, CAS7:1 becomes WE7:1.

TABLE 5-5. DISPLAY MEMORY CONNECTIONS

5.7 MULTIPLEXED HOST BUS CONNECTIONS

The following tables list the multiplexed host interface groups. Most of the signals connected to pins in these groups depend upon which host group is selected. Connections are listed for the following groups: VESA VL-Bus and PCI Bus.

PIN NO.	SIGNAL NAME(1)	I/O	DESCRIPTION
110, 130-127, 117-119, 108-104, 102, 100- 97, 95-93, 91-87, 85-81	AD31:0(2)	I/O	Multiplexed Host Address/data
80, 79	D1:0	I/O	Host Data
69	$\overline{ADS}$	I	Address/Data Strobe
67, 68, 80, 79	$\overline{BE}$3:0	I	Byte Enables
64	IRQ9	O	Interrupt Request
66	LCLK	I	CPU clock
77	$\overline{LDEV}$	O	Device Selected
71	$\overline{LRDY}$	O	Local Bus Ready (to Host)
78	M/$\overline{IO}$	I	Memory or I/O Cycle Status
70	$\overline{RDYRTN}$	I	Ready Return (from Host)
65	$\overline{RESET}$	I	System Reset
74	W/$\overline{R}$	I	Write or Read Cycle Status

NOTES:

(1) Signal names are derived from VESA VL-Bus specification

(2) Multiplexed bus connections are listed. The de-multiplexed VL-Bus uses A23:2, $\overline{ADRM}$, $\overline{ADRZ}$, and D31:0. Refer to Table 5-9.

TABLE 5-6. VESA VL-BUS CONNECTIONS

PIN NO.	SIGNAL NAME(1)	I/O	DESCRIPTION
110, 130-127, 117-119, 108-104, 102, 100- 97, 95-93, 91-87, 85-81	AD31:0(2)	I/O	Multiplexed Host Address/data
78	$\overline{\text{CHIPKILL}}$	I	Turn off WD9710
66	CLK	I	PCI-bus Clock
65	$\overline{\text{RST}}$	I	System Reset
67, 68, 75, 76	C/$\overline{\text{BE3:0}}$	I	Bus Command/ Byte Enables
69	$\overline{\text{FRAME}}$	I	Cycle Frame
71	$\overline{\text{TRDY}}$	O	Target Ready
70	$\overline{\text{IRDY}}$	I	Initiator Ready
74	$\overline{\text{STOP}}$	O	Stop
121	PAR	O	Parity
122	IDSEL	I	Initialization Device Select
73	$\overline{\text{DEVSEL}}$	O	Device Select
64	$\overline{\text{IRQ}}$	O	Interrupt Request

NOTES:

(1) Signal names are derived from PCI Local Bus specification 2.0

(2) Some PCI bus connections are multiplexed with connections for the VL-bus. Refer to Table 5-8

TABLE 5-7. PCI-BUS CONNECTIONS

5.8 HOST INTERFACE SHARED PINS

Table 5-8 and 5-9 list the signals that share common pins on the host interface bus. The active signals depend on which bus has been selected. Table 5-9 lists the signal names on the shared pins of the host interface. For the VESA VL-bus, multiplexed signals are listed on the left of the reverse virgule (\) and de-multiplexed signals are listed to the right of the virgule. Where no virgule appears, the same signal is used in either case.

Table 5-9 lists the signals on the shared pins of the multiplexed VAFC and RAMDAC connectors and the equivalent pins on the de-multiplexed host interface. Where two or more signals are listed for the same pin, the signal name are separated by a reverse virgule (\). To determine specific applications, refer to Table 5-4

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PIN NO.	I/O	VL-BUS (47 PINS)	PCI-BUS (46 PINS)
110	I/O	AD31\ D31	AD31
112-115, 117-119	I/O	AD30:24\D30:24	AD30:24
108-104, 100, 99	I/O	AD23:16\A23:16	AD23:16
98, 97, 95-93, 91-87, 85-81	I/O	AD15:2\ A15:2	AD15:2
80	I	D1\$\overline{\text{ADRM}}$	AD1
79	I	D0\$\overline{\text{ADRZ}}$	AD0
75	I	$\overline{\text{ADS}}$	$\overline{\text{FRAME}}$
73	I	$\overline{\text{BE3}}$	C/$\overline{\text{BE3}}$
74	I	$\overline{\text{BE2}}$	C/$\overline{\text{BE2}}$
81	I	$\overline{\text{BE1}}$	C/$\overline{\text{BE1}}$
82	I	$\overline{\text{BE0}}$	C/$\overline{\text{BE0}}$
64	O	IRQ9	IRQ
71	I	LCLK	CLK
79	O	$\overline{\text{LDEV}}$	$\overline{\text{DEVSEL}}$
132	I/O	$\overline{\text{LRDY}}$	$\overline{\text{TRDY}}$
84	I	M/$\overline{\text{IO}}$	$\overline{\text{CHIPKILL}}$
76	I	$\overline{\text{RDYRTN}}$	$\overline{\text{IRDY}}$
70	I	$\overline{\text{RESET}}$	$\overline{\text{RST}}$
80	I	W/$\overline{\text{R}}$ (R=O)	$\overline{\text{STOP}}$ (O)
122	0	$\overline{\text{EABUF}}$\ DAT23	$\overline{\text{PAR}}$
148	0	$\overline{\text{EDBUF}}$\ DAT22	$\overline{\text{IDSEL}}$
149	0	BUFDIR\ DAT21	---

TABLE 5-8. HOST INTERFACE SHARED PINS

PIN NO.	MULTIPLEXED HOST BUS				DE-MULTIPLEXED HOST BUS			
	WITH VAFC CONNECTOR (52 PINS)		16-BIT RAMDAC (56-PINS)		VL-BUS (56-PINS)		AT BUS (56-PINS)	
	SIGNAL	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL	I/O
121	$\overline{\text{EABUF}}$	O	$\overline{\text{EABUF}}$	O	D23	I/O	---	---
122	$\overline{\text{EDBUF}}$	O	$\overline{\text{EDBUF}}$	O	D22	I/O	---	---
123	BUFDIR	O	BUFDIR	O	D21	I/O	---	---
124	$\overline{\text{BLANK}}$	I/O	$\overline{\text{BLANK}}$	I/O	D20	I/O	---	---
125	$\overline{\text{RPTL}}$\MVCLK	O	$\overline{\text{RPTL}}$\MVCLK	O	D19	I/O	---	---
126	$\overline{\text{WPTL}}$\GRDY	O	$\overline{\text{WPTL}}$\GRDY	O	D18	I/O	---	---
127	$\overline{\text{EXVID7}}$	O	$\overline{\text{EXVID}}$	O	D17	I/O	---	---
128	PCLK\DCLK	I/O	PCLK\DCLK	I/O	D16	I/O	---	---
130	WCLK\VID15	I/O	WCLK\VID15	O	D15	I/O	D15	I/O
131	$\overline{\text{EXPCLK}}$\VID14	I/O	VID14	O	D14	I/O	D14	I/O
132	$\overline{\text{EXSYNC}}$\VID13	I/O	VID13	O	D13	I/O	D13	I/O
133	VID12	---	VID12	O	D12	I/O	D12	I/O
134	VID11	---	VID11	O	D11	I/O	D11	I/O
135	VID10	---	VID10	O	D10	I/O	D10	I/O
136	VID9	---	VID9	O	D09	I/O	D9	I/O
137	VID8/VIDS	O	VID8/VIDS	O	D08	I/O	D8	I/O
139	VID7	I/O	VID7	I/O	D07	I/O	D7	I/O
140	VID6	I/O	VID6	I/O	D06	I/O	D6	I/O
141	VID5	I/O	VID5	I/O	D05	I/O	D5	I/O
142	VID4	I/O	VID4	I/O	D04	I/O	D4	I/O
143	VID3	I/O	VID3	I/O	D03	I/O	D3	I/O
144	VID2	I/O	VID2	I/O	D02	I/O	D2	I/O
145	VID1	I/O	VID1	I/O	D01	I/O	D1	I/O
146	VID0	I/O	VID0	I	D00	I/O	D0	I/O
110	AD31	I/O	---	---	D31	---	$\overline{\text{SRDY}}$	O
112-115	AD30:27	I	---	---	D30:27	---	---	I/O
117-119	AD26:24	I	---	---	D26:24	---	---	I/O
108-104, 102, 100, 99	AD23:16	I	SLA23:16	I	A23:16	I	SLA23:16	I/O
98, 97, 95-93, 91-87, 85, 84, 83, 82	AD15:02	I	AD15:02	I	A15:2	I	SLA15:2	I
80	D1	I	AD1	I	$\overline{\text{ADRM}}$	I	SLA1	I
79	D0	I	AD0	I	$\overline{\text{ADRZ}}$	I	SLA0	I

NOTE: On the PCI bus, PAR shares a pin with $\overline{\text{EABUF}}$ and IDSEL shares a pin with $\overline{\text{EDBUF}}$.

TABLE 5-9. HOST INTERFACE/VAFC CONECTOR/RAMDAC SHARED PINS

5.9 DISPLAY MEMORY BUS SHARED CONNECTIONS

The following table lists the functions of the display memory connector pins for dual-$\overline{CAS}$ and dual $\overline{WE}$ display memory configurations.

PIN NO.	DRAM DUAL-CAS (86-PINS)	I/O	DRAM DUAL-WE (86-PINS)	I/O
8-11, 13, 14, 17-20	MA9:0	O	MA9:0	O
22, 7	$\overline{RAS1:0}$	O	$\overline{RAS1:0}$	O
63	$\overline{CAS7}$	O	$\overline{WE7}$	O
53	$\overline{CAS6}$	O	$\overline{WE6}$	O
42	$\overline{CAS5}$	O	$\overline{WE5}$	O
32	$\overline{CAS4}$	O	$\overline{WE4}$	O
175	$\overline{CAS3}$	O	$\overline{WE3}$	O
184	$\overline{CAS2}$	O	$\overline{WE2}$	O
195	$\overline{CAS1}$	I/O	$\overline{WE1}$	I/O
6	$\overline{CAS0}$	I/O	$\overline{CAS0}$	I/O
15	$\overline{WE}$	O	$\overline{WE}$	O
21	$\overline{OE}$	O	$\overline{OE}$	O
62-55, 52-49, 47-44, 41-34, 31-28, 26-23	MD63:32	I/O	MD63:32	I/O
176-183, 186-189, 191-194, 196-203, 205-208, 2-5	MD31:0	I/O	MD31:0	I/O

TABLE 5-10. DISPLAY MEMORY BUS SHARED PINS

5.10 EXTERNAL COMPONENT CONNECTOR PINS

Table 5-11 lists the signals for connecting optional external devices to the display memory data bus. Depending upon the memory configuration, one of more of the external devices can be attached at the same time.

PIN NO.	I/O	SIGNAL	RAMDAC	ROM	PCLK
205-208, 2-5	I/O	MD7:0	---	Q7:0	EXT CLK SEL 5:0
196-203	I/O	MD15:8	D7:0	---	---
176-183, 186-189, 191-194	I/O	MD31:16	RS1:0 (1)	A15(2):0	---

NOTE:

(1) RAMDAC pin RS2, if present, should be grounded

(2) For 32K ROM, bit A15 is not connected

TABLE 5-11. EXTERNAL DEVICE CONNECTIONS

5.11 MONITOR/VAFC/CLOCK CONNECTIONS

The following signals provide the interface to the internal RAMDAC, monitor, external RAMDAC and VAFC connector, and the clock generator. All pins are not available in every configuration.

PIN NO.	SIGNAL	I/O	DESCRIPTION
INTERNAL RAMDAC			
196-203	D7:0	I/O	Internal RAMDAC Data
193, 194	RS1:0	I/O	Internal RAMDAC Row Select
155	R (analog)	AO	Internal RAMDAC Red Output
152	G (analog)	AO	Internal RAMDAC Green Output
149	B (analog)	AO	Internal RAMDAC Blue Output
151	RSET(1)	AI	Internal RAMDAC Full-scale Control
153	VREF (analog)	AI	Internal RAMDAC Voltage Reference
157	RVCC	---	Power to Internal RAM
148	RVSS	---	Internal RAM Grounds
156	DVCC	---	Power to Internal DAC
150, 154	DVSS	---	Internal DAC Grounds
MONITOR			
161	HSYNC±	I/O	Horizontal Sync
160	VSYNC±	I/O	Vertical Sync
EXTERNAL RAMDAC/VAFC CONNECTOR			
139-146	VID7:0	I/O	Video Output to Palette/Data In for VAFC Connector
130-136	VID15:9	O	Video Output to Palette/Data In for VAFC Connector
137	VIDS\ VID8	O	Enable VID7:0\ Video Output to Palette/Data In for VAFC Connector
128	PCLK\ DCLK	I/O	Pixel Clock to Palette/Master Clock to VAFC Connector
124	$\overline{\text{BLANK}}$	I/O	Blank for RAMDAC/ Screen Blank for VAFC Connector
125	$\overline{\text{RPLT}}$\ MVCLK	O	Palette Read Strobe/ Video Clock for VAFC Connector
126	$\overline{\text{WPLT}}$\ GRDY	O	Palette Write Strobe/ Graphics Ready for VAFC Connector
151	MDET(1)	I	External RAMDAC Monitor Detect
127	$\overline{\text{EXVID}}$	I	VAFC Connector Video Enable
207, 208, 2-5	EXTCLK SEL5:0	0	External Clock Select
CLOCK GENERATOR			
168	MCLK	I	Master Clock
172	VCLK	I	Video Clock
130	WCLK	O	Clock Generator Write Strobe
169	MCAP	AI	Master Clock Analog Input
171	VCAP	AI	Video Clock Analog Input
170	CVCC	---	Power Supply for Clock Generator
173	CVSS	---	Clock Generator Ground

NOTES:

(1) $\overline{\text{RSET}}$ and $\overline{\text{MDET}}$ share the same pin.

(2) AO and AI indicate an analog output and analog input, respectively.

TABLE 5-12. MONITOR/VAFC/CLOCK CONNECTIONS

TABLE 5-12. MONITOR/VAFC/CLOCK CONNECTIONS (Continued)

5.12 MISCELLANEOUS CONTROL CONNECTIONS

The following signals control miscellaneous functions of the WD9710.

PIN NO.	SIGNAL	I/O	DESCRIPTION
121	$\overline{\text{EABUF}}$	O	Enable Address Buffer
122	$\overline{\text{EDBUF}}$	O	Enable Data Buffer
123	BUFDIR	O	Data Buffer Direction
163	$\overline{\text{EBROM}}$	O	Enable BIOS ROM
205-208, 2-5	Q7:0	I/O	ROM Data
176-183, 186-189, 191-194	A15:0	I/O	ROM Address
166	USR0	O	User Programmable Bit 0
165	USR1	O	User Programmable Bit 1
164	USR2	O	User Programmable Bit 2
159	USR3	O	User Programmable Bit 3
158	USR4	O	User Programmable Bit 4

TABLE 5-13. MISCELLANEOUS CONTROL PINS

5.13 POWER AND GROUND CONNECTIONS

The following table provides an alphabetical listing of the power and ground connections. For descriptions of each signal, refer to Table 5-2.

PIN NO.	NAME	FUNCTION
170	CVCC	Power to Internal clock
173	CVSS	Ground for internal clock power
156	DVCC	Power to Internal DAC
150, 154	DVSS	Ground for internal DAC power
157	RVCC	Power to Internal RAM
148	RVSS	Ground for internal RAM power
12, 27, 48, 72, 83, 92, 101, 111, 120, 138, 167, 185, 204	VCC	Main Power to Core Logic
1, 16, 33, 43, 54, 77, 86, 96, 103, 109, 116, 129, 147, 162, 174, 190	VSS	Ground VSS = 0V

TABLE 5-14. POWER AND GROUND CONNECTIONS

6.0 REGISTER ACCESS

6.1 OVERVIEW

All of the WD9710 enhanced functions are controlled by one or more registers, most of which are in addition to standard VGA registers.

Additionally, most VGA registers have an alternate mapping into the enhanced register space.

These enhanced function registers are designed for 16-bit access, but also support 32-bit access.

Enhanced functions are controlled by indexed register blocks. Each indexed register block contains up to fifteen 12-bit indexed registers. The 4-bit register index is written along with the 12-bit data field to form a 16-bit word. A few register blocks contain other than 12-bit registers. These can hold up to 240 8-bit or three 14-bit registers.

6.2 ACCESSING INDEXED REGISTERS

All enhanced function registers are accessed through the Register Access port. To write to one or more indexed registers within any register block, the register block must be first be selected by loading its address into the Register Block Pointer field of the Index Control register. The Index Control Access bit must be 0 for this to occur. This causes the selected register block to appear at the Register Access port.

6.3 REGISTER ACCESS PORT

The *Register Access* port is a 16- or 32-bit port that is used to read and write all extended registers. All individual transfers through the port are 16 bits and 32-bit operations are split into two 16-bit transfers.

The *Register Access* port defaults on reset to the 23CXh I/O space, or may be re-mapped through configuration bits to 63CXh, A3CXh, or E3CXh. It may also be re-mapped by software into the B8XX Xh memory space.

6.4 INDEX CONTROL REGISTER

The Index Control register is a read-write register that controls reads and writes to indexed registers blocks. It is written as follows:

BITS	INDEX F(1)
D15:12	1111 (index)
D11:8	Register read index, bits 3:0(2)
D7	Index control access
D6	Auto-increment
D5:0	Register block pointer(3)
D3:0	Register read index, bits 7:4(4)

NOTE:

(1) This registers appears at Index F in all register blocks

(2) When read, this field returns the index of the register to be read next

(3) When bit 7 is a 0

(4) When bit 7 is a 1

TABLE 6-1. INDEX Fh CONTROL REGISTER

D6	REGISTER ACCESS MODE
1	Auto-increment disabled
0	Auto-increment enabled

D7	INDEX CONTROL ACCESS
1	Set 8 bits of read-back index only
0	Set register block pointer and 4 bits of read-back index

6.5 WRITING EXTENDED REGISTERS

After selecting the register block containing the desired registers, a 16-bit word is written to the Register Access port.

To write a 12-bit indexed register, the 4 high-order bits specify the index of the individual register being written, while the 12 low-order bits are the data to be written. Additional registers within the same register block may then be written without re-selecting that register block.

To write an 8-bit indexed register, the 8 high-order bits specify the index, while the 8 low-order bits specify the data. To write a 14-bit register, the 2 high-order bits specify the index, and the 14 low-order bits specify the data.

6.6 READING EXTENDED REGISTERS

To read one or more indexed registers within a register block, the address of that register block and the index of the desired register are first written to the Register Block Pointer and Register Read Index fields respectively of the Index Control register. The Index Control Access bit must be 0 to load the Register Block Pointer. This causes the selected register to appear at the Register Access port.

When register blocks have more than 15 registers, this method may be used to access the first 15 registers of the register blocks. To access a higher-indexed register directly, a write to the Index Control register is followed by a second write to the Index Control register with the Index Control Access bit set to 1, which loads all 8 bits of the read-back index. Alternatively, a register above index Eh can be reached through auto-increment.

A 16-bit word is then read from the Register Access port. When reading an indexed register, the value returned contains the index of the register in the 2, 4, or 8 high-order bits, depending on the type of register block.

If the auto-increment feature is not enabled, consecutive reads to the Register Access port returns the same register. This is useful for checking the status of operations in progress.

6.7 CHAIN READS

If the Auto-Increment feature is enabled, consecutive reads to the Register Access port returns consecutively indexed registers within the same register block. Registers are read in ascending order through the highest-numbered register in the block. The next read causes the Register Block Pointer to be incremented automatically, and read its return index Fh along with the new Register Block Pointer value.

If this next register block exists, it is returned on subsequent reads. If it does not exist, the next read again increments the Register Block Pointer and returns index Fh with its new value.

After the Register Block Pointer has reached all 1's, it is not incremented on subsequent reads. In this manner, a chain read is implemented that reads register values until index 1 of the highest possible register block (3F) is returned. Since it is not incremented on subsequent reads, it can be searched for in the high word on 32-bit reads, where it appears even if it also appears in the low word of the same read.

In this manner, the long chain of registers returned by a sequence of reads to the Register Access port can be later written back as they were to the same port to facilitate save/restore operations.

6.8 CHAIN WRITES

The host may load most of the chip's registers by a chain write to the Register Access port. This is accomplished by simply concatenating writes to different register blocks, using the write to index Fh (or similar) to switch between different blocks.

The chain read function has been specifically design to permit a context save/restore to be accomplished simply by writing back the entire list returned during the chain read in a chain write operation.

6.9 CONTEXT SWITCHING

Certain operations, such as interrupt-driven cursor updates and context switching, require the host to read back the complete index control register, including the full 8-bit read-back index. This is accomplished through a special register block 3Fh. This register block contains two read-only registers returning the current Register Block Pointer and current read-back Index. These registers returned the values as they were **latched immediately before entry to this register block**, and are formatted for easy write-back at a later time, by simply setting the high nibble of each word to Fh and writing to the Register Access Port. These registers are as follows:

BITS	FUNCTION
D15:12	0000 (index)
D11:8	Register Read Index, bits 3:0(1)
D7	0
D6	Auto-increment
D5:0	Register Block Pointer(2)

NOTE:

(1) When read, this field returns the index of the register to be read next

(2) These bits return the value that was latched just prior to entering this mode.

TABLE 6-2. INDEX CONTROL 0, R/O BLOCK 3F INDEX 0

BITS	FUNCTION
D15:12	0001 (index)
D11:8	Register Read Index, bits 3:0(1)
D7	1
D6:4	000
D3:0	Register Read Index, bits 7:4(2)

NOTE:

(1) When read, this field returns the index of the register to be read next

(2) These bits return the value that was latched just prior to entering this mode.

TABLE 6-3. INDEX CONTROL 1, R/O BLOCK 3F INDEX 1

6.10 VGA REGISTER READS AND WRITES

VGA registers can be written and read through the normal VGA ports. Most of these registers can also be read through the Register Access port.

Each of the VGA register groups (3C0/1, 3C4/5, 3CE/F, and 3?4/5) have a register block pointer address. The registers can be accessed just like normal 8-bit extended registers.

NOTE

While the physical data registers are the same, the VGA index registers (such as 3C4h) are not affected by reads or writes through the Register Access port.

6.11 REGISTER OPERATIONS (32-BIT)

It is possible to access the Register Access port as a 32-bit port to read or write two 16-bit registers at a time.

When writing two 16-bit registers at a time, the register accessed by the low word is written first, followed by the high word. This ordering is especially important when one of the register writes either starts an operation or modifies the Register Block Pointer.

If the low word of a 32-bit register write starts an operation, the register write in the high word holds pending completion of the operation.

When reading two 16-bit registers at a time, the first 16-bit register is returned in the low word, and the second in the high word. This ordering is especially important when one of the registers returns index Fh with its new Register Block Pointer value. Note that when auto-increment is disabled, both words return the same register.

7.0 HARDWARE CURSOR

7.1 OVERVIEW

The Hardware Cursor supports a user-defined pattern of up to 64 by 64 pixels, defined at 2 bits per pixel. The cursor pattern should be stored in a non-visible part of display memory. The cursor operates in all graphics modes, as well as VGA text modes. The Hardware Cursor register block is accessed via I/O port 23C8h.

7.2 REGISTER MAP

INDEX	FUNCTION
0	Cursor Control
1	Cursor Pattern Address Low
2	Cursor Pattern Address High
3	Cursor Primary Color
4	Cursor Secondary Color
5	Cursor Origin
6	Cursor Display Position X
7	Cursor Display Position Y
8	Cursor Auxiliary Color
9:E	Reserved
F	Cursor Register Read Control

TABLE 7-1. CURSOR REGISTER, BLOCK 9

7.3 CURSOR REGISTER READ CONTROL

The Cursor Register Read Control register is used to set the index value for reading the Hardware Cursor registers.

BITS	FUNCTION
D15:12	1111 (index)
D11:8	Cursor Register Read Index
D7:0	Reserved

TABLE 7-2. CURSOR REGISTER READ CONTROL, INDEX F

7.4 CURSOR CONTROL REGISTER

The Cursor Control register controls operation of the hardware cursor.

BITS	FUNCTION
D15:12	0000 (index)
D11	Cursor enable (refer to Note)
D10:9	Cursor pattern type (must be 01)
D8	Cursor Plane Protection
D7:5	Cursor mode
D4	Not Used
D3	Cursor color format
D2:0	Not Used
NOTE: Bit D11 is reset during power turn-on and reset.	

TABLE 7-3. CURSOR CONTROL, INDEX 0

D11	CURSOR ENABLE
1	Cursor is displayed
0	Cursor is not displayed

D10	D9	CURSOR PATTERN TYPE
1	1	Cursor is a 64-wide vertical stripe
0	1	Cursor is 2 bits per pixel, 64 by 64 pixels

D8	CURSOR PLANE PROTECTION
1	Cursor Plane Protection Enable
0	Cursor Plane Protection Disable

D7	D6	D5	CURSOR MODE
0	1	1	Three-color Cursor
0	1	0	Two-color Cursor with Special Inversion
0	0	1	Two-color Cursor with Inversion
0	0	0	Straight Monochrome (compatibility)

D3	CURSOR COLOR FORMAT
1	Cursor color values are direct
0	Cursor color values are indexed

7.5 CURSOR PATTERN ADDRESS AND ORIGIN

BITS	FUNCTION
D15:12	0001 (index)
D11:0	Cursor pattern address bits 11:0[1][2]

NOTE:

(1) Must be on a 64-bit boundary

(2) Bits D11:0 are reset during power turn-on and reset

TABLE 7-4. CURSOR PATTERN ADDRESS LOW, INDEX 1

BITS	FUNCTION
D15:12	0010 (index)
D11:10	Not Used
D9:0	Cursor pattern address bits 21:12

NOTE:

Bits D9:0 are reset during power turn-on and reset

TABLE 7-5. CURSOR PATTERN ADDRESS HIGH, INDEX 2

The two Cursor Pattern Address registers form a 22-bit byte address which specifies the location in the non-visible portion of display memory where the first byte of the cursor pattern is stored. This value is independent of the cursor origin. The cursor pattern must be stored on a 64-bit (8 byte) boundary.

Generally, this address represents the CPU address where the pattern begins minus the CPU address of the top-left corner of the display memory.

BITS	FUNCTION
D15:12	0101 (index)
D11:6	Cursor origin Y (0-63)
D5:0	Cursor origin X (0-63)

NOTE:

Bits D11:0 are reset during power turn-on and reset

TABLE 7-6. CURSOR ORIGIN, INDEX 5

The Cursor Origin register specifies the offset from the top-left corner of the pattern that is displayed at the cursor display position. This value is often referred to as the cursor's "hot spot".

NOTE

A write to either of the Cursor Pattern Address Registers or to the Cursor Origin register does not take effect until the beginning of a video frame following the next write to the Cursor Control register. In Interlaced mode, the effect occurs in the next video field.

7.6 CURSOR DISPLAY POSITION

BITS	FUNCTION
D15:12	0110 (index)
D11	Not Used
D10:0	Cursor display position X[1][2]

NOTE:

(1) This register is written differently in 9-dot character mode

(2) Bits D10:0 are reset during power turn-on and reset

TABLE 7-7. CURSOR DISPLAY POSITION X, INDEX 6

BITS	FUNCTION
D15:12	0111 (index)
D11	Not Used
D10:0	Cursor display position Y
NOTE: Bits D10:0 are reset during power turn-on and reset	

TABLE 7-8. CURSOR DISPLAY POSITION Y, INDEX 7

The Cursor Display Position X and Y registers specify the location on the screen where the cursor origin is displayed. These values represent a position in pixels, referenced to the top-left corner of the screen, regardless of the display mode.

In text modes, the cursor position still represents pixels, not characters The cursor can be displayed at any position on the screen, including between characters.

In 9-dot text mode, the cursor position is stored in a special manner, as follows

BITS	FUNCTION
D15:12	0110 (index)
D11,2:0	Cursor display position X, in pixels(1)
D10:3	Cursor display position X, in characters
NOTE: (1) Legal values are 0 8	

TABLE 7-9. CURSOR DISPLAY POSITION X (9-DOT MODE), INDEX 6

NOTE

Any write to the Cursor Display Position X or Y register takes effect at the beginning of the next video frame (In interlaced mode, the next video field)

7.7 CURSOR COLOR REGISTERS

The cursor color registers control display of the 2-bit per pixel cursor patterns.

BITS	FUNCTION
D15:12	0011 (index)
D11:8	Not Used
D7:0	Cursor primary color

TABLE 7-10. CURSOR PRIMARY COLOR, INDEX 3

BITS	FUNCTION
D15:12	0100 (index)
D7:0	Cursor secondary color

TABLE 7-11. CURSOR SECONDARY COLOR, INDEX 4

BITS	FUNCTION
D15:12	1000 (index)
D11:8	Not Used
D7:0	Cursor auxiliary color

TABLE 7-12. CURSOR AUXILIARY COLOR, INDEX 8

The Cursor Primary Color, Cursor Secondary Color, and Cursor Auxiliary Color registers specify eight-bit cursor color values. The Cursor Color Format bit of the Cursor Control register specifies whether these values represent indexed or direct colors.

When applying indexed colors in 256-color mode, these values are applied as 8-bit pixels.When applying indexed colors in 16-color mode, the Cursor Palette Select bit in the Cursor Control register selects whether the cursor is applied using 4-bit or 8-bit colors. In the former case, only the low nibble of each color is applied, and the result is passed through the attribute controller's palette. In the latter case, cursor pixels are applied as 8 bit colors and those pixels are not processed through the internal palette.

In direct color modes, these values represent direct colors as follows:

BITS	FUNCTION
D7:6	Red, 3 most significant bits
D5:2	Green, 3 most significant bits
D1:0	Blue color, 2 most significant bits
NOTE: The remaining low-order bits of each color are duplicates of the high-order bits.	

TABLE 7-13. CURSOR EXTENDED COLOR MAPPING

7.8 REGISTER UPDATES

When a new cursor pattern is being selected, up to four different registers must be updated. If a new video frame were to begin before all registers were updated, a single frame could be displayed with incorrect cursor data. While the display would recover within one video frame, the results would be visually annoying.

Therefore, the WD9710 incorporates circuitry to hold off use of updated register data until all of the associated registers have been updated.

Following any write to either the Cursor Pattern Address or the Cursor Origin register, the current frame is always completed with the previous register values. Therefore, the Cursor Control register must be written after updating any of these registers, even if the data in it is to remain unchanged. However, reads to any of these registers always return the data last written to the register, whether or not such data has already taken effect. Normally, all of these writes take place within a single frame, and the new cursor is drawn on the following frame.

Any write to the Cursor Display Position X or Y registers takes effect after the beginning of the next video frame.

In interlaced mode, updates of the above registers occur at the beginning of a video field rather than frame.

7.9 CURSOR ADDRESS MAPPING

Cursor patterns are usually stored in contiguous, non-visible locations of display memory. In some modes, regions that are made to appear contiguous to the CPU or the BITBLT hardware are in fact fragmented. The host must be certain to load the cursor pattern in physically contiguous memory locations.

CPU(1)(2) ADDRESS	CURSOR PATTERN ADDRESS
PAGE 0	
A0000	0 ... *If pattern starts here...*
A0001	n(3)... *then next byte is here...*
A0002	n(3)... *then here...*
A0003	n(3)... *then here...*
A0004	n(3) ... *then here...*
A0005	n(3) ... *then here...*
A0006	n(3)... *then here...*
A0007	n(3) ... *then here...*
A0008	8 ... *and ninth byte is here*
⇓	⇓
AFFFC	FFFC
PAGE 1	
A0000	10000
⇓	⇓

NOTES:

(1) CPU addresses are shown for VGA mode 13 or similar

(2) These locations are usually visible. In practice, cursor pattern is usually stored in non-visible memory

(3) Cursor pattern must start on a 64-bit boundary, but the pattern is stored using all bytes (n).

TABLE 7-14. CPU ADDRESS TO CURSOR ADDRESS MAPPING

7.10 TWO-BIT CURSOR PATTERN FORMAT

The cursor pattern pointed to by the Cursor Pattern Address registers for two-bit cursor patterns is stored in consecutive 1 Kbyte memory locations. The following table defines how cursor pattern data is stored.

OFFSET	FUNCTION
0(1)	Cursor pattern, AND mask, row 0, columns 0-7(2)
1	Cursor pattern, XOR mask, row 0, columns 0-7
2	Cursor pattern, AND mask, row 0, columns 8-15
⇓	⇓
15	Cursor pattern, XOR mask, row 0, columns 56-63
16	Cursor pattern, AND mask, row 1, columns 0-7
⇓	⇓
1023	Cursor pattern, XOR mask, row 63, columns 56-63

NOTE:

(1) Offset is in bytes from cursor pattern starting location

(2) Within each byte, the high-order bit represents the left-most pixel

TABLE 7-15. CURSOR PATTERN - 2-BIT PER PIXEL

7.11 LOADING THE CURSOR PATTERN

Loading a cursor pattern requires writing the pattern to a non-visible portion of display memory and then pointing to the pattern with the Cursor Pattern Address registers. A cursor pattern already in display memory can be selected simply by loading these registers.

7.12 CURSOR COLOR MODES

A cursor may be displayed using any of four color modes, selected by the Cursor Color Mode field of the Cursor Control register. Depending on the color mode selected, each 2-bit pixel of the cursor pattern is displayed against the background described in the following table.

CURSOR PATTERN(1)	COLOR MODE			
	0	1	2	3
0 0	all 0's	sec	sec	sec
0 1	all 1's	pri	pri	pri
1 0	trans	trans	trans	trans
1 1	inv	inv	spec(2)	aux

NOTES:

(1) The high-order bit of each 2-bit pattern is the AND mask, the low-order bit is the XOR mask.

(2) Background is XOR'd with the auxiliary color and then inverted.

LEGEND:

sec = secondary, pri = primary, trans = transparent, inv = inverted, spec = special inversion, aux = auxiliary

TABLE 7-16. CURSOR COLOR MODES

The special inversion generates the inverse of the destination exclusive-OR'ed with the auxiliary color register. This retains the "different from background" color property of inversion while adding the ability to specify a "preferred" inversion color which is displayed for any desired background color.

To use this feature, the Cursor Color Mode field must be set to "special inversion", and the Cursor Auxiliary Color should be loaded with the exclusive-NOR (XNOR) of the background color to be translated and the desired color to be displayed. When set, any screen pixel of the former color covered by an inverting cursor pattern pixel is "inverted" into the auxiliary color.

7.13 CURSORS OVER A MOTION VIDEO WINDOW

When a cursor is fully or partially within a motion video window, the cursor is applied normally, using the color mode and formats of the cursor, and ignoring the color mode of the motion video window. However, any inverted pixel in a cursor pattern falling over a motion video window is displayed using the cursor auxiliary color.

7.14 VERTICAL CURSOR STRIPE

When the Cursor Pattern Type field of the Cursor Control register is set to 11, the cursor is displayed as a vertical stripe, 64 pixels wide, starting from its normally specified location and continuing to the bottom of the screen. This feature is intended to provide a pop-up, icon stripe that is useful for displaying status information.

8.0 HARDWARE CLIPPING

8.1 OVERVIEW

The Hardware Clipping function supports clipped drawing engine writes inside or outside of any rectangular region in display memory. When enabled, the clipping function simply masks write operations within (or outside of) the clipping region. Clipping does not apply to VGA or motion video port writes.

8.2 REGISTER MAP

INDEX	FUNCTION
0	Clipping Control
1	Not Used
2	Clipping Boundary Left
3	Clipping Boundary Right
4	Clipping Boundary Top
5	Clipping Boundary Bottom

TABLE 8-1. CLIPPING REGISTERS, BLOCK 3

8.3 CLIPPING CONTROL REGISTER

The Clipping Control register controls operation of the clipping function.

BITS	FUNCTION
D15:12	0000 (index)
D11:4	Not Used
D3	Clipping abort enable
D2	Clipping interrupt enable
D1	Clipping polarity
D0	Clipping enable
NOTE: Bit D0 is reset during power turn-on and reset	

TABLE 8-2. CLIPPING CONTROL, BLOCK 3 INDEX 0

D3	CLIPPING ABORT ENABLE
1	Abort drawing operations under certain clipping conditions
0	Do not abort drawing engine operations due to clipping

D2	CLIPPING INTERRUPT ENABLE
1	Interrupt on any write outside clipping area
0	No interrupt on writes outside clipping area

D1	CLIPPING POLARITY
1	Writes inside clipping boundary inhibited
0	Writes outside clipping boundary inhibited

D0	CLIPPING ENABLE
1	Clipping is enabled
0	Clipping is disabled

8.4 CLIPPING BOUNDARY REGISTERS

The following registers define the clipping boundary. All dimensions are in pixels relative to the top left corner of display memory (which is not necessarily the same as the visible screen). The edges of the region containing the specified pixels include the top and left boundaries and exclude the right and bottom boundaries.

BITS	FUNCTION
D15:12	0010 (index)
D11:0	Clipping boundary left

TABLE 8-3. CLIPPING BOUNDARY LEFT, BLOCK 3 INDEX 2

BITS	FUNCTION
D15:12	0011 (index)
D11:0	Clipping boundary right

TABLE 8-4. CLIPPING BOUNDARY RIGHT, BLOCK 3 INDEX 3

BITS	FUNCTION
D15:12	0100 (index)
D11:0	Clipping boundary top

TABLE 8-5. CLIPPING BOUNDARY TOP, BLOCK 3 INDEX 4

BITS	FUNCTION
D15:12	0101 (index)
D11:0	Clipping boundary bottom

TABLE 8-6. CLIPPING BOUNDARY BOTTOM, BLOCK 3 INDEX 5

8.5 CLIPPING ABORT

When the Clipping Abort Enable bit is set in the Clipping Control register, the drawing engine operations terminate automatically once certain clipping criteria are met. Of course, even with this option set, a drawing engine operation may terminate due to completion of its requested drawing operation.

BITBLT operations terminate when the vertical component of the destination makes the transition from inside to outside the clipping region. If a BITBLT operation (which includes rectangles and patterns) begins vertically outside of the clipping region, the operation terminates after the operation enters and then leaves the vertical clipping region.

Vector operations terminate when the vector being drawn makes the transition from inside to outside the clipping region.

Clipping and clipping abort do not apply to VGA writes.

9.0 HARDWARE BITBLT

9.1 OVERVIEW

The BITBLT hardware supports accelerated transfers of data between regions of display memory, or between system and display memory.

A BITBLT operation consists of exactly one command and zero or more operators. Each operator is independent and may be enabled or disabled for each command. Some combinations of operators may not be available or useful for a given command.

BITBLT commands include, in addition to conventional BITBLT, rectangle fills, and pattern fills. The hardware also supports vector draw, described in detail in another chapter.

BITBLT operators include raster operations, plane and byte masking, source and destination transparency, scan fills, and color expansion with or without transparency.

Most BLIT operations can also be performed to or from the host, using a mode known as "Host BLIT".

The BITBLT hardware supports, 8-bit, 15-bit, 16-bit color and 24-bit color modes, and can also be used in text modes. There is also limited support for 4-bit color modes.

9.2 BITBLT REGISTER MAP

INDEX	FUNCTION(1)
0	BITBLT Control - part 1 (Refer to Section 9.24)
1	BITBLT Control - part 2
2	BITBLT Source X/Low
3	BITBLT Source Y/High
4	BITBLT Destination X/Low(1)
5	BITBLT Destination Y/High(1)
6	BITBLT Dimension X
7	BITBLT Dimension Y
8	BITBLT Source Row Pitch
9	BITBLT Destination Row Pitch
A	BITBLT Logical Operations
B	BITBLT Vertical Stretch Factor (Refer to Section 9.19)

NOTE:
(1) All or part of these registers can change automatically

TABLE 9-1. FIRST BITBLT REGISTER BLOCK (BLOCK 4)

TABLE 9-1. FIRST BITBLT REGISTER BLOCK (BLOCK 4) (Continued)

INDEX	FUNCTION
0	BITBLT Foreground Color low/Blue
1	BITBLT Foreground Color high/Green
2	BITBLT Background Color low/Blue
3	BITBLT Background Color high/Green
4	BITBLT Foreground Color Red
5	BITBLT Background Color Red
6	BITBLT Transparency Color low/Blue
7	BITBLT Transparency Color high/ Green
8	BITBLT Transparency Color Red/Mask Low
9	BITBLT Transparency Mask High
A	BITBLT Plane Mask low
B	BITBLT Plane Mask high
C	BITBLT Byte Mask

TABLE 9-2. SECOND BITBLT REGISTER BLOCK (BLOCK 5)

9.3 SOURCE AND DESTINATION

The BITBLT Source X/Low and BITBLT Source Y/High registers specify the source address for BITBLT operations. The BITBLT Destination X/Low and BITBLT Destination Y/High registers specify the destination address.

When rectangular (X/Y) addressing is used, the X and Y terms are specified in pixels. When linear addressing is used, the high and low fields of each register pair are concatenated to form a 22-bit pixel address pointing to the top-left corner of the source or destination area.

When linear addressing is used and the source and destination areas overlap in certain ways, BITBLT must be started from the opposite corner to prevent parts of the source area from being overwritten by the destination array before they are copied. In this case, the host specifies the lower-right corner of the source and destination regions and sets the BITBLT Direction bit in the BITBLT Control register.

BITS	FUNCTION
D15:12	0010 (index)
D11:0	BITBLT source position X(1)
D10:0	BITBLT source position - bits 10:0(2)

NOTE:

(1) This value is in pixels when X/Y addressing is used.

(2) This value is in pixels when linear addressing is used.

TABLE 9-3. BITBLT SOURCE X/LOW, BLOCK 4 INDEX 2

BITS	FUNCTION
D15 12	0011 (index)
D11 0	BITBLT source position Y(1)
D11 0	BITBLT source position - bits 22:11(2)

NOTE:

(1) This value is in pixels when X/Y addressing is used.

(2) This value is in pixels when linear addressing is used.

TABLE 9-4. BITBLT SOURCE Y/HIGH, BLOCK 4 INDEX 3

BITS	FUNCTION
D15:12	0100 (index)
D11:0	BITBLT destination position X(1) auto update
D11:0	BITBLT destination position - bits 10:0(2) *auto update*

NOTE:

(1) This value is in pixels when X/Y addressing is used.

(2) This value is in pixels when linear addressing is used.

TABLE 9-5. BITBLT DESTINATION X/LOW, BLOCK 4 INDEX 4

BITS	FUNCTION
D15:12	0101 (index)
D11:0	BITBLT destination position Y(1) auto update
D11:0	BITBLT destination position - bits 22:11(2) *auto update*

NOTE:

(1) This value is in pixels when X/Y addressing is used.

(2) This value is in pixels when linear addressing is used.

TABLE 9-6. BITBLT DESTINATION Y/HIGH, BLOCK 4 INDEX 5

9.4 DIMENSIONS

The BITBLT Dimension X register specifies the width of the rectangular region to be copied. This value is expressed in pixels in both the rectangular and linear addressing modes.

The BITBLT Dimension Y register specifies the height of the rectangular region to be copied. This value is always expressed in pixels. **When vertical stretching is in effect (refer to Section 9.19), this register specifies the height of the destination region.**

BITS	FUNCTION
D15:12	0110 (index)
D11:0 .	BITBLT dimension X
NOTE: The legal range of dimension X is 0 to 4K-1 pixels	

TABLE 9-7. BITBLT DIMENSION X, BLOCK 4 INDEX 6

BITS	FUNCTION
D15:12	0111 (index)
D11:0	BITBLT dimension Y
NOTE: The legal range of dimension Y is 0 to 4K-1 pixels	

TABLE 9-8. BITBLT DIMENSION Y, BLOCK 4 INDEX 7

9.5 ROW PITCH

The BITBLT Source and Destination Row Pitch registers specify the offsets between vertically adjacent pixels for the source and destination respectively. This value is expressed in pixels.

To copy a rectangular region to a contiguous space, which is useful for storing an on-screen region in off-screen memory, the destination row pitch should be set equal to the value in the BITBLT Dimension X register. Similarly, to copy a contiguous space to a rectangular region, the source row pitch should be set equal to the value in the BITBLT Dimension X register. The above methods can be combined to copy one contiguous region to another.

BITS	FUNCTION
D15:12	1000 (index)
D11:0	BITBLT source row pitch, in pixels

TABLE 9-9. BITBLT SOURCE ROW PITCH BLOCK 4 INDEX 8

BITS	FUNCTION
D15:12	1001 (index)
D11:0	BITBLT destination row pitch, in pixels

TABLE 9-10. BITBLT DESTINATION ROW PITCH, BLOCK 4 INDEX 9

9.6 LOGICAL OPERATIONS

The BITBLT Logical Operation register specifies a logical bit operation to be performed on the source and destination fields. This field is always active, and must be loaded with the appropriate value even when a simple source copy is being performed.

BITS	FUNCTION
D15:12	1010 (index)
D11:8	BITBLT raster operation
D7:6	BITBLT scan fill select
D5:4	Not Used
D3	BITBLT monochrome transparency
D2	BITBLT transparency polarity
D1:0	BITBLT transparency select
NOTE: Bit D2 has a different meaning when scan fills are enabled	

TABLE 9-11. BITBLT LOGICAL OPERATIONS, BLOCK 4 INDEX A

D11:8	BITBLT RASTER OPERATION
NOTE: Refer to Table 9-13.	

D7	D6	BITBLT SCAN FILL SELECT
0	X	Scan fill is not enabled
1	0	Reserved
1	1	Destination pixels control scan fill

D3	BITBLT MONOCHROME TRANSPARENCY
1	Monochrome transparency is enabled
0	Monochrome transparency is not enabled

D2	BITBLT TRANSPARENCY POLARITY
1	Matching pixels are opaque
0	Matching pixels are transparent
NOTE: Bit D2 has a different meaning when scan fills are enabled	

D1	D0	BITBLT TRANSPARENCY SELECT
1	1	Destination pixels control transparency
1	0	Source pixels control transparency
0	X	Transparency is not enabled

9.7 BITBLT RASTER OPERATION

The BITBLT Raster Operation specifies a logical operation to be performed on the source and destination fields. These fields are always active and must be loaded with the appropriate value even when a simple source copy is to be performed.

All BITBLT operations apply a source color, pattern, or area to a destination region. The result, which is written to the destination, is a logical function of the source and destination pixels for each location.

The Raster Operation code is defined as follows:

The source (S) and Destination (D) form a 2-bit value. Table 9-12 lists the logical results of these combined Source and Destination values.

The four 1-bit results from Table 9-13 form the Raster Operation code (abcd). The 'a' in the code is defined as the high order bit.

While the Raster Operation code represents a two-input operation (any two results form one code), both inputs are not always relevant to the operation. For example, codes 0011 (source copy) and 1100 (inverted source copy) are independent of the destination value.

NOTE

Arithmetic operations are not supported.

S	D	RESULT
0	0	a
0	1	b
1	0	c
1	1	d

TABLE 9-12. RESULTS OF COMBINED SOURCE AND DESTINATION VALUES

RASTER OP CODE (abcd)	FUNCTION	RASTER OP CODE (abcd)	FUNCTION
0000	Zero	1000	NOR
0001	AND	1001	XNOR
0010	$S \bullet \overline{D}$	1010	Inverted Destination
0011	Source	1011	$S+\overline{D}$
0100	$\overline{S} \bullet D$	1100	Inverted Source
0101	Destination	1101	$\overline{S}+D$
0110	XOR	1110	NAND
0111	OR	1111	One

TABLE 9-13. RASTER OPERATION CODE FUNCTIONS

9.8 FOREGROUND AND BACKGROUND COLORS

BITS	FUNCTION
D15:12	0000 (index)
D11:8	Not Used
D7:0	BITBLT foreground color - bits 7:0/ Blue

TABLE 9-14. BITBLT FOREGROUND COLOR LOW/BLUE, BLOCK 5 INDEX 0

BITS	FUNCTION
D15:12	0001 (index)
D11:8	Not Used
D7:0	BITBLT foreground color - bits 15:8/Green

TABLE 9-15. BITBLT FOREGROUND COLOR HIGH/GREEN, BLOCK 5 INDEX 1

BITS	FUNCTION
D15:12	0100 (index)
D11:8	Not Used
D7:0	BITBLT foreground color red

TABLE 9-16. BITBLT FOREGROUND COLOR RED, BLOCK 5 INDEX 4

BITS	FUNCTION
D15:12	0010 (index)
D11:8	Not Used
D7:0	BITBLT background color - bits 7:0/Blue

TABLE 9-17. BITBLT BACKGROUND COLOR LOW/BLUE, BLOCK 5 INDEX 2

BITS	FUNCTION
D15:12	0011 (index)
D11:8	Not Used
D7:0	BITBLT background color - bits 15:8/Green

TABLE 9-18. BITBLT BACKGROUND COLOR HIGH/GREEN, BLOCK 5 INDEX 3

BITS	FUNCTION
D15:12	0101 (index)
D11:8	Not Used
D7:0	BITBLT background color red

TABLE 9-19. BITBLT BACKGROUND COLOR RED, BLOCK 5 INDEX 5

The BITBLT Foreground and Background Color registers specify 8- 16- or 24-bit colors to be used when expanding monochrome source areas. The foreground color is also used to specify the color of a filled rectangle.

9.9 COLOR TRANSPARENCY

Color transparency is the concept that a certain color or range of colors in the source or destination field of a BITBLT are actually "transparent", with the rest being "opaque". Transparent source colors do not overwrite the background. Opaque destination colors cannot be overwritten. A common simplified form of source transparency is the logical OR of source and destination, in which a source field of zero is effectively a transparent color since it does not change the destination when OR'ed with it.

Color source and destination transparency are both supported, but only one or the other may be in effect at any one time. Monochrome source transparency can be in effect by itself or with destination transparency.

BITS	FUNCTION
D15:12	0110 (index)
D11:8	Not Used
D7:0	BITBLT transparency color - bits 7:0/Blue

TABLE 9-20. BITBLT TRANSPARENCY COLOR LOW/BLUE, BLOCK 5 INDEX 6

BITS	FUNCTION
D15:12	0111 (index)
D11:8	Not Used
D7:0	BITBLT transparency color - bits 15:8/Green

TABLE 9-21. BITBLT TRANSPARENCY COLOR HIGH/GREEN, BLOCK 5 INDEX 7

BITS	FUNCTION
D15:12	1000 (index)
D11:8	Not Used
D7:0	BITBLT transparency color Red/ transparency mask - bits 7:0

TABLE 9-22. BITBLT TRANSPARENCY COLOR RED/MASK LOW, BLOCK 5 INDEX 8

BITS	FUNCTION
D15:12	1001 (index)
D11:8	Not Used
D7:0	BITBLT transparency mask - bits 15:8
D2	BITBLT transparency mask - red component
D1	BITBLT transparency mask - green component
D0	BITBLT transparency mask - blue component
NOTE: Bits D1:0 are used in direct color modes	

TABLE 9-23. BITBLT TRANSPARENCY MASK HIGH, BLOCK 5 INDEX 9

The BITBLT Transparency Color registers specifies a 8-, 16- or 24-bit color to be used as the transparency color. The BITBLT Transparency Mask register specifies a mask for use in comparison against the transparency color.

The pixels of the destination are compared against the transparency color under control of the transparency mask. Each bit of the transparency mask that is a '1' makes the corresponding bit or field of the transparency color bit a "don't care".

The BITBLT Transparency Select field of the BITBLT Logical Operations register specifies whether color transparency is enabled, and if so, whether the source or destination region controls transparency. The BITBLT Transparency Polarity bit specifies whether pixels matching the transparency color are considered transparent, in which case the destination at that location is not overwritten, or opaque, in which case pixels not matching the transparency color cause the background not to be overwritten.

Monochrome transparency operates independently of color transparency, and is **described elsewhere in this document.**

9.10 PLANE AND BYTE MASKS

BITS	FUNCTION
D15:12	1010 (index)
D11:8	Not Used
D7:0	BITBLT plane mask - bits 7:0

TABLE 9-24. BITBLT PLANE MASK LOW, BLOCK 5 INDEX A

BITS	FUNCTION
D15:12	1011 (index)
D11:8	Not Used
D7:0	BITBLT plane mask - bits 15:8

TABLE 9-25. BITBLT PLANE MASK HIGH, BLOCK 5 INDEX B

BITS	FUNCTION
D15:12	1100 (index)
D11:8	Not Used
D7:0	BITBLT byte mask - bytes 7:0

TABLE 9-26. BITBLT BYTE MASK, BLOCK 5 INDEX C

The BITBLT Plane Mask registers specify a mask that inhibits writing of certain planes within the destination region. The BITBLT Byte Mask register specifies a mask that inhibits writing of certain bytes in display memory. The byte mask refers to aligned 64-bit regions.

When any bit in these register is zero, the corresponding plane or byte of the destination region, if applicable to the destination region, is not modified during any BITBLT operation. These masks have no effect on other than drawing engine operations.

9.11 ADDRESS MAPPING

In all modes, the source and destination addresses are pixel addresses. Addresses represent the pixel at the top-left corner of the respective region.

REGISTER ADDRESS	DISPLAY MEMORY LOCATION
1	2nd pixel of display memory (1 or more bytes)
0	1st pixel of display memory (1 or more bytes)

TABLE 9-27. BITBLT ADDRESS MAPPING

For example, in 256-color mode, where display memory starts at CPU address A0000h, CPU address A0456h would correspond to register address 456h. In 16-bit per pixel mode, CPU address A0456 would correspond to register address 22Bh. Where display memory is divided into pages, the location is calculated as if all pages were consecutive. For example, with display memory pages of 64K bytes, CPU address A0123h in the second page of display memory would correspond to register value 10123h in 256-color mode.

9.12 MONOCHROME TO COLOR EXPANSION

When the source of a BITBLT operation is monochrome, each '0' in the source region is replaced with the specified background color, while each '1' is replaced with the foreground color. All other processing options, including masks and raster operations remain active and operate on the expanded colors.

When the source of a BITBLT operation is monochrome and the BITBLT Monochrome Transparency bit is set in the BITBLT Logical Operations register, each '1' in the source is replaced with the foreground color, while each '0' does not cause the destination to be updated.

All monochrome source regions must start on a 32-bit boundary. They may have any length in pixels. When a monochrome source region is linearly mapped, each row of the pattern is padded to an integral number of 32-bit words.

9.13 SCAN FILLS

Scan fills can be used to quickly generate filled polygons on the screen. This is accomplished by drawing a partial outline of the polygon in an otherwise unused color, specifying a bounding rectangle for the polygon, and applying the scan fill operation to a rectangle command.

The BITBLT Scan Fill Select field of the BITBLT Logical Operations register specifies whether scan fill is enabled, and if so, whether the source or destination region controls scan fills.

When destination scan fills are enabled, each line of the destination region is scanned from left to right while it is being written. Each pixel is compared against the BITBLT Transparency Color and BITBLT Transparency Mask registers. Destination update is not enabled until the first pixel which matches the transparency color, and is toggled on every subsequent matching pixel. Filling is enabled in the region between **and including** the two matching pixels. Even though a group of consecutive pixels may all match the transparency color, each is checked individually and can toggle the scan fill. This would often be used with the Filled Rectangle command to quickly fill an area already outlined. The toggle is reset at the beginning of each scan line.

The BITBLT Transparency Polarity bit has a special meaning when scan fills are enabled. Scan fills are always toggled when the transparency color is matched. Unlike other operations, this bit does not invert the result of the comparison. Instead, the bit specifies whether each new

scan line begins with filling enabled or disabled, as follows:

D2	BITBLT TRANSPARENCY POLARITY
1	Scan filling enabled at left edge of bounding rectangle
0	Scan filling disabled at left edge of bounding rectangle
NOTE: This bit has a different meaning when scan fills are disabled.	

Scan filling is not available with overlapping source and destination.

9.14 FILLED RECTANGLES

To generate a filled rectangle, the BITBLT Command field of the BITBLT Control register is set to Rectangle, and the BITBLT Foreground Color register to the desired fill color. A source address is not required. All other BITBLT operators are available normally.

9.15 PATTERNS

The pattern command may be used to accelerate the copying of 8 by 8 or 16 by 16 source patterns. In this mode, a full-color pattern can be repetitively "tiled" to a large destination area in an efficient manner.

To perform a pattern copy, the host writes the desired pattern to display memory in a linear fashion as defined below. The host then loads the BITBLT Source registers with the location of the pixel within the pattern corresponding to the top-left corner of the destination region. The Pattern command must be specified in the BITBLT Command field of the BITBLT Control register.

The pattern requires from 64 bytes (for an 8 by 8 pattern in 8-bit color mode) to 1024 bytes (for a 16 by 16 pattern in a 32-bit color mode). The pattern must be stored in display memory in a region aligned to its size. Note that while the pattern represents a rectangular area it is stored in a linear fashion using consecutive bytes in an aligned region. The source address, however, must point to the pixel within the region to be anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point.

All pattern are always aligned the top-left corner of display memory, and not to the destination region of the current BLIT operation. In this way, a non-rectangular region that is composed of many rectangular swatches, which may have been written at different times, does not show any seams where the swatches come together.

For this reason, the low-order bits of the source register, which represent the row and column within the pattern where the destination starts being written, must correspond to the modulo 8 or 16 row and column address of the destination. Patterns should not be written from right-to-left.

9.16 PATTERN STORAGE EXAMPLE

In 256-color mode, an 8 by 8 source pattern is stored in display memory in a 64-byte aligned area. It is stored as 64 consecutive bytes, not as a rectangular region. When performing the pattern copy, however, the source address may point to any pixel within the 64-pixel region. This pixel is anchored to the top-left corner of the destination region, and the pattern wraps to the right and down from that point.

ADDRESS	DISPLAY MEMORY CONTENTS
⇩	⇩
n-2	(any data)
n(1)	Top row of pattern, left-most pixel
n+1(2)	Top row of pattern, second pixel
⇩	⇩
n+7	Top row of pattern, right-most pixel
n+8	Second row of pattern, left-most pixel
⇩	⇩
n+63	Bottom row of pattern, right-most pixel
n+64	(any data)
⇩	⇩
NOTE: (1) The 'n' must be a multiple of 64 pixels (2) The addresses are given in pixels	

TABLE 9-28. BITBLT PATTERN STORAGE

The addresses given in Table 9-29 are correct for 8 by 8 patterns. The addresses for 16 by 16 patterns would extend from 'n' to 'n+255'. For 16-bit or 32-bit per pixel patterns, each address represents the appropriate number of bits.

9.17 STRIP DRAW

The WD9710 incorporates strip draw functionality for highly efficient drawing of one-pixel wide lines. These are intended for host-assisted drawing of trapezoids, run-length-encoded (RLE) images, and strip-drawn vectors.

In all strip-draw cases, the operation is started by writing the BITBLT Dimension X register, which draws a one-pixel high strip using the current BITBLT Foreground Color of the specified number of pixels. All normal BITBLT operations are available, but the BITBLT Dimension Y is assumed to be 1. The destination registers are automatically updated depending on the specific BITBLT operation being performed.

When the "RLE" command is selected in the BITBLT Command register, the WD9710 is configured for drawing run-length encoded images. At the end of a strip draw, the destination is set to the pixel immediately to the right of the last pixel in the previous strip. Generally, the host sets the BITBLT Foreground Color followed by the X Dimension to generate a strip. Between rows, the host may set the BITBLT Destination registers directly.

When the "Trapezoid fill" command is selected in the BITBLT Command register, the WD9710 is configured for host-assisted trapezoid fill. At the end of a strip draw, the destination is set to the pixel immediately below the first pixel in the previous strip. Generally, the host corrects the BITBLT Destination X, if necessary, and then sets the BITBLT Dimension X to generate a strip.

When the "strip vector" command is selected in the BITBLT Command register, the WD9710 is configured for host-assisted strip line draw. The BITBLT Direction bit of the BITBLT Command register specifies whether strips are drawn left-to-right or right-to-left, and the destination is set to the column immediately to the right or left of the endpoint, respectively. The endpoint row is either one row below or one row above the current row depending on the setting of the BITBLT Parameter.

Generally, the host sends a series of values to the BITBLT Dimension X to generate a strip line.

9.18 VERTICAL STRIP DRAW

When the Vertical Strip Draw command is selected in the BITBLT Control register (Control 1 bits 4:0 = 01x00), the WD9710 is configured for a highly-efficient single-pixel wide vertical strip. The length of the vertical strip is selected by the BITBLT Dimension Y register. This operation assumes a value of 1 in the BITBLT Dimension X register.

The vertical strip draw is usually slower than a horizontal strip draw of comparable length. Also, a vertical strip draw can be performed using the filled rectangle operation; however, such operations are not as efficient.

9.19 STRETCH BLIT

Stretch BLIT is a BITBLT variant that copies a rectangular source area to a rectangular destination area of the same width but a different height. If the destination is of a larger height than the source, selected source rows are replicated to fill the required number of destination rows. If the destination is of a smaller height then the source, selected source rows are not copied.

To perform a stretch BLIT, the BITBLT Stretch bit is set in the BITBLT Control register (refer to Section 9.24), and the vertical stretch factor is loaded into the BITBLT Vertical Stretch Factor register. This factor is calculated by dividing the destination height by the source height and normalizing to 040h. In other words, a stretch factor of 080h represents a 2:1 stretch, while a factor of 020h represents a 2:1 shrink.

BIT	FUNCTION
D15:12	1011 (index)
D11:0	BITBLT vertical stretch factor

TABLE 9-29. BITBLT VERTICAL STRETCH FACTOR, BLOCK 4 INDEX B

Generally, the source and destination of a stretch BLIT should not overlap. This is because in certain cases of overlap, neither top-to-bottom nor bottom-to-top operation can avoid having the destination writes overwrite as-yet unread source areas. Stretch BLIT is ignored on areas that do not have a source region specified.

9.20 VENETIAN BLIT

Venetian BLIT is a special type of stretch BLIT specifically aimed at motion video. In this operation, the host is responsible for stretching the image horizontally, and the WD9710 stretches the image in the vertical direction.

In venetian BLIT, the host writes one copy of each horizontal line, as it would in a stretch BLIT. In a normal stretch BLIT, the host writes the source into a contiguous off-screen region, which then becomes the source of the stretch BLIT. Alternatively, a rectangular region may be stretched vertically into a different rectangular region.

In a venetian BLIT, however, the host writes each line into the stretched region of display memory where it appears. Some lines in the destination appear more than once, but the host writes only the first occurrence of each line. The venetian BLIT operation fills in the missing lines.

Venetian BLIT derives its speed from the fact that the first line of each replicated group does not have to be copied from a source to a destination, and that it takes no longer for the host to write data to the correct destination than it does to write data to a contiguous off-screen region.

To properly execute a venetian BLIT, the host must use the same DDA stretch algorithm as does the WD9710, so that the first row of each replicated group is written to the locations expected by the WD9710.

NOTE

The BITBLT Vertical Scale Factor register is set for venetian BLIT to a value of 40h less than the corresponding stretch factor for a normal stretch BLIT.

9.21 HOST BLITS FROM SYSTEM MEMORY TO DISPLAY MEMORY

To transfer data quickly from system memory to display memory, the host may set up a BITBLT operation with the source coming from the host through a system memory or I/O location and the destination in display memory. Acceleration is provided by the WD9710 handling the rotation and merging of the data. This operation is also known as a "host write BLIT".

After starting the BITBLT operation, the host writes a series of words or double words to the Host BLIT port, which may be an I/O port or memory mapped. It may be accessed either 16 or 32 bits at a time. One line of the source is transferred at a time, and each line is padded to an integral number of 64-bit words.

When the host attempts to write data faster than the WD9710 can handle it, the WD9710 holds off the host. Similarly, when a host BLIT operation requires data from the host that is not yet available, the operation is suspended until data becomes available.

Therefore, the host must send exactly the correct amount of data for each host BLIT, otherwise the system may hang. The correct data to send for any host BLIT consists of all words containing any of the pixels to be copied.

Just like the destination, the source region may have any alignment. The 3 low-order bits of the BITBLT Source X/Low register specify the pixel alignment of the source region. The other bits of the register may have any value. In the same manner as a source region in display memory, the low-order bits of the register specify the position of the start of the source region within the first 64-bit word written. In this manner, the host may perform only aligned transfers to display memory, even though the source region is not always aligned to a word or double-word boundary.

Even though the source of a host-BLIT operation is not in display memory, the BITBLT Source Row Pitch register is still used and must be set correctly. The contents of this register are added to the source value as in a normal BITBLT at the end of each line. This permits the "first pixel" pointed to be the source register to change automatically

from line to line, which is extremely useful when the source width is not a multiple of four bytes, and consecutive scan lines, while always word aligned, are not double-word aligned and the left edge of the region "slides" within a double word from scan line to scan line.

Just like display memory, no source double word from the host may straddle two lines of the destination. In cases when a double word in system memory does straddle two lines of the source region, that double word must be sent twice; once as the last word of the first line, then again as the first word of the second line.

All operators are available in host-BLIT mode. Patterns cannot be generated from the host without substantial driver assistance.

9.22 HOST BLITS FROM DISPLAY MEMORY TO SYSTEM MEMORY

To transfer data quickly from display memory to system memory, the host may set up a BITBLT operation with the destination going to the host through a system memory or I/O location and the source in display memory. This operation is very similar to a host BLIT from system memory to display memory, and is also known as a "host read BLIT".

In a host read BLIT, the host reads from the Host BLIT port, which may be an I/O location or memory-mapped. The 3 low-order bits of the BITBLT Destination X/Low register specify the byte location within the first double-word read corresponding to the left edge of the destination. Note that unlike host BLIT writes, the host is responsible for protecting any pixels from change at the left and right boundaries of the destination if copying the read data into system memory.

The host must read exactly the correct number of 64-bit words from the WD9710. This requires reading any double word that contains one or more pixels of the source region.

Most operators are not available in a host read BLIT, because these operators require either a read-modify-write of the destination, or write-protection control on individual bits or pixels in the destination.

9.23 HOST BLITS FROM SYSTEM MEMORY TO DISPLAY MEMORY WITH COLOR EXPANSION

To transfer monochrome data quickly from system memory to display memory, the host may set up a host write BLIT with color expansion.

In this operation, all 1's in the source are replaced by a pixel of the foreground color and all 0's are either replaced by a pixel or the background color or are transparent, depending on the value of the BITBLT Monochrome Transparency bit in the BITBLT Logical Operations register.

The BITBLT Source X/Low register points to the byte within the first double word corresponding to the left edge of the source region. As in screen-to-screen BLITs, all monochrome source regions must be byte aligned.

9.24 CONTROL AND STATUS

BITS	FUNCTION
D15:12	0000 (index)
D11	BITBLT activation(2)
D10	BITBLT direction(1)
D9	Venetian BLIT
D8	BITBLT destination color
D7	Enable 8-bit Pattern
D6	BITBLT source color
D5	Stretch BLIT
D4:0	BITBLT command

NOTES:

(1) This bit is ignored and the correct value calculated automatically when X/Y addressing is used

(2) This bit is automatically reset when BITBLT is completed. Since a read to this register is held until the BITBLT completes, it always returns 0

TABLE 9-30. BITBLT CONTROL - PART 1, BLOCK 4 INDEX 0

D11	BITBLT ACTIVATION
1	Begin BITBLT / Begin host BLIT
0	Do not begin BITBLT/Abort host BLIT

D10	BITBLT DIRECTION
1	BITBLT direction is right-to-left, bottom-to-top
0	BITBLT direction is left-to-right, top-to-bottom

NOTE:
This bit is ignored and the BITBLT direction is calculated internally when X/Y addressing is used.

D9	VENETIAN BLIT
1	Venetian BLIT enabled
0	Venetian BLIT disabled

D8	BITBLT DESTINATION COLOR
1	Destination is monochrome
0	Destination is color

D7	ENABLE 8-BIT PATTERN
1	Pattern Enabled
0	Pattern Disabled

D6	BITBLT SOURCE COLOR
1	Source is monochrome
0	Source is color

D5	STRETCH BLIT
1	Vertical Stretch Enabled
0	Vertical Stretch Disabled

D4	D3	D2	D1	D0	BITBLT COMMAND
1	0	0	1		Host BLIT read
1	0	0	0		Host BLIT write
0	1	y	x	x	Strip draw - vector
0	0	1	1	1	Strip draw - trapezoid fill
0	0	1	1	0	Strip draw - RLE
0	0	1	0	1	16 by 16 Pattern
0	0	1	0	0	8 by 8 Pattern
0	0	0	1	---	Rectangle Fill
0	0	0	0	---	BITBLT

NOTES:
y = 0: positive direction along y-axis.
y = 1: negative direction along y-axis.
xx = 00: no movement along x-axis.
xx = 01: positive direction along x-axis.
xx = 10: negative direction along x-axis.
Other values are reserved for other operations or for future expansion.

BITS	FUNCTION
D15:12	0001 (index)
D11	BITBLT interrupt enable
D10	BITBLT quick start
D9	BITBLT update destination
D8:6	Not Used
D5	BITBLT Source/Destination Linear Map
D4:3	BITBLT pixel depth
D2:0	BITBLT row width

TABLE 9-31. BITBLT CONTROL - PART 2 BLOCK 4 INDEX 1

D11	BITBLT INTERRUPT ENABLE
0	Do not interrupt on completion of BITBLT
1	Interrupt on completion of BITBLT

D10	BITBLT QUICK START
0	BITBLT starts only when explicitly enabled
1	BITBLT starts automatically when certain registers are written

D9	BITBLT UPDATE DESTINATION
0	Do not update destination on completion of BITBLT
1	Update destination on completion of BITBLT

D5	BITBLT SOURCE/DESTINATION LINEAR MAP
0	Specified area is rectangular in display memory
1	Specified area is linear in display memory

D4	D3	BITBLT PIXEL DEPTH
0	0	Reserved
0	1	8 bits per pixel
1	0	16 bits per pixel
1	1	32 bits per pixel

D2	D1	D0	BITBLT ROW WIDTH
1	1	1	2048 pixel wide X,Y X/Y addressing
1	1	0	1600 pixel wide X,Y addressing
1	0	1	1280 pixel wide X,Y addressing
1	0	0	1024 pixel wide X,Y addressing
0	1	1	800 pixel wide addressing
0	1	0	640 pixel wide X,Y addressing
0	0	1	320 pixel wide X,Y addressing
0	0	0	Linear addressing mode (addresses in pixels x resolution = 11 bits y resolution = 12 bits)

9.25 LINEAR AND X/Y ADDRESSING

All BITBLT operations may be performed using linear or X/Y addressing. When the BITBLT Row Width field in the BITBLT Control register is set to 000, linear addressing is selected. Otherwise, X/Y addressing is selected.

In linear addressing, all source and destination addresses and the X dimension are expressed in pixels. When the source and destination regions overlap, the BITBLT Direction bit must be set correctly in the BITBLT Control register, and the BITBLT Source and Destination registers must sometimes point to the lower-right corner of their respective regions.

In X/Y addressing, all source and destination addresses and dimensions are expressed in pixels.

When the host X/Y addressing is selected, the BITBLT Row Width field is automatically used to specify the width of each logical row in display memory.

9.26 AUTOMATIC DESTINATION UPDATE

A host doing multiple BITBLTs need only update those registers that change from one BITBLT to the next. Most BITBLT registers never change unless written by the host. The exceptions to this rule are the two BITBLT Destination registers.

When the BITBLT Update Destination bit in the BITBLT Control register is set, the BITBLT Destination registers are automatically updated at the end of each BITBLT operation to point to the pixel immediately to the right of the top-right corner of the previous destination region, except as noted below. This is specifically aimed at improving text output operations.

When the drawing operation is a strip draw for trapezoid fill and destination update is enabled, the destination is left pointing to the pixel immediately below the starting pixel for the last operation. This is intended to accelerate trapezoid fills, as the Y destination is almost certainly updated correctly, and the X destination is probably updated correctly.

When the drawing operation is a strip vector, the destination is left one pixel to the right of, and one pixel above or below, the ending pixel of the last operation, depending on the BITBLT Parameter field.

9.27 QUICK START MODE

When the BITBLT Quick Start bit is set in the BITBLT Control register, BITBLT starts automatically when certain registers are written. The BITBLT operation starts with the values currently loaded into the BITBLT Control register.

The register whose write automatically starts a BITBLT is selected according to the following criteria, in this order:

1. Filled rectangles or strip draw: the BITBLT Dimension X register.
2. Automatic destination update selected: the BITBLT Source Low/X register.
3. Otherwise: the BITBLT Destination low/X register.

This mode permits a chain of BITBLT operations to be performed with one less register write operation than would otherwise be required. All other bits in the BITBLT Control register operate as they were last written, and the BITBLT Activation bit is physically set and can be read back normally.

9.28 ABORTED BITBLT

The host may abort a BITBLT in progress by writing the Device Status register with the Drawing Engine Status bit reset. The operation then terminates within a few memory clocks.

When a BITBLT is aborted, the destination registers are generally unchanged, unless the operation was coincidentally aborted near the very end.

Aborted BITBLTs cannot be continued, since it is unknown what remains to be copied, and even if it were known, the region remaining to be copied might not be rectangular. Further, BITBLTs that use certain logical operations or transparency settings might not produce correct results if simply repeated with the original parameters.

10.0 VECTORS

10.1 OVERVIEW

The WD9710 is capable of drawing vectors anywhere in display memory. Vectors are drawn between any two points in display memory.

10.2 REGISTER MAP

Registers for vector operations are spread across multiple register blocks. One of these register blocks is specific to vectors, the other two register blocks are overlaid on the BITBLT register blocks.

INDEX	FUNCTION
OVERLAID ON FIRST BITBLT REGISTER BLOCK (BLOCK 4)	
0	Vector Control - part 1(1)
1	Vector Control - part 2
2	Not Used(3)
3	Not Used(3)
4	Vector Start X(1)
5	Vector Start Y(1)
6	Vector Length
7	Not Used(3)
8	Vector Vertical Row Pitch(2)
9	Vector Horizontal Row Pitch(2)
A	Vector Logical Operations
B	Vector Byte mask(2)
OVERLAID ON SECOND BITBLT REGISTER BLOCK (BLOCK 5)	
0	Vector Foreground Color low/Blue(2)
1	Vector Foreground Color high/Green(2)
2	Not Used(3)
3	Not Used(3)
4	Vector Foreground Color Red(2)
5	Not Used(3)
6	Vector Transparency Color low/Blue(2)
7	Vector Transparency Color high/ Green(2)
8	Vector Transparency /Red(2)
9	Vector Transparency Mask(2)
A	Vector Plane Mask low(2)
B	Vector Plane Mask high(2)
VECTOR REGISTERS (BLOCK 7)	
0(4)	Vector orthogonal constant
1	Vector diagonal constant
2	Vector initial error constant

NOTE:

(1) All or part of these registers can change automatically.

(2) These register functions are unchanged from BITBLT operations, and therefore are not described in the following paragraphs.

(3) However, writing these locations would still overwrite the underlying BITBLT register location.

(4) For vector registers, the index is the top two bits of register access port only. Therefore, the register block contains only three registers. For changing the register block pointer, the host should still write to the register access port with all four high-order bits set to 1.

TABLE 10-1. VECTORS REGISTERS (Continued)

10.3 VECTOR START POSITIONS AND PIXEL COUNTS

The Vector Start X and Y registers specify the starting location of the vector. These must be expressed in X/Y coordinates.

BITS	FUNCTION
D15:12	0100 (index)
D11:0	Vector Start X

TABLE 10-2. VECTOR START X, BLOCK 4 INDEX 4

BITS	FUNCTION
D15:12	0101 (index)
D11:0	Vector Start Y

TABLE 10-3. VECTOR START Y, BLOCK 4 INDEX 5

BITS	FUNCTION
D15:12	0110 (index)
D11:0	Vector length
NOTE: The Vector Length register specifies the vector length in pixels.	

TABLE 10-4. VECTOR LENGTH, BLOCK 4 INDEX 6

10.4 LOGICAL OPERATIONS FOR VECTORS

The Vector Logical Operations register is available but is more restrictive than its BITBLT counterpart. Source transparency and scan fills are not available. Monochrome transparency is implied in any vector fill operation.

10.5 VECTOR CONTROL

BITS	FUNCTION
D15 12	0000 (index)
D11	Vector activation(1)(2)
D10 8	Not Used
D9 7	Vector direction
D4 0	Vector parameter

NOTE

(1) Bit D11 is automatically reset when the vector is completed. Since a read to this register is held until the vector completes, it always returns 0.

(2) Bit D11 is reset during power turn-on and reset

TABLE 10-5. VECTOR CONTROL - PART 1, BLOCK 4 INDEX 0

D11	VECTOR ACTIVATION
1	Begin vector
0	Do not begin vector

D9	D8	D7	VECTOR DIRECTION
X	X	1	Y-step is negative
X	X	0	Y-step is positive
X	1	X	X-step is negative
X	0	X	X-step is positive
1	X	X	Major axis is Y
0	X	X	Major axis is X

D4	D3	D2	D1	D0	VECTOR PARAMETER
1	1	0	0	---	Vector
---	---	---	---	1	Do not draw last pixel
---	---	---	---	0	Draw last pixel
NOTE: Other values are reserved for other operations or for future expansion					

BITS	FUNCTION
D15:12	0001 (index)
D11	Vector interrupt enable
D10	Vector quick start
D9	Vector update destination
D8:0	Not Used
NOTE: Bit D11 is reset during power turn-on and reset	

TABLE 10-6. VECTOR CONTROL - PART 2, BLOCK 4 INDEX 1

D11	VECTOR INTERRUPT ENABLE
1	Interrupt on completion of vector
0	Do not interrupt on completion of vector

D10	VECTOR QUICK START
1	Vector starts automatically when destination register is written, or when the source register is written if the destination update is enabled.
0	Vector starts only when explicitly enabled

D9	VECTOR UPDATE DESTINATION
1	Update destination on completion of vector
0	Do not update destination on completion of vector

10.6 VECTOR DIRECTION AND LAST PIXEL CONTROL

To generate a vector, the host specifies the major axis and X and Y directions of the vector or vectors to be generated. The major axis of a vector is the axis on which each pixel of the vector is at a different position. The X-step of a vector is the direction in which the vector moves projected along the X-axis. The Y-step is the direction in which it moves projected along the Y-axis. When a vector is completely horizontal or vertical, one of these axes shows no movement and the corresponding bit can have any value.

When the Vector Parameter field in the Vector Control register is set to 1, the last pixel of the line is not drawn, but is still calculated.

10.7 VECTOR UPDATE DESTINATION AND QUICK START

The vector update destination and vector quick start fields work similarly to their BITBLT counterparts, except that when the *Vector Update Destination* bit is set in the *Vector Control* register, the *Vector Start X* and *Y* registers are loaded with the position of the last pixel in the specified line. This value is the same whether or not the last pixel is drawn, and is also unaffected by other parameters, such as masking and transparency, that may cause parts of the line not to update the destination.

10.8 VECTOR DDA VALUES

Generation of vectors requires calculation of certain DDA values by the host. Each vector requires three such values to be loaded into the 14-bit registers in the Vector register blocks. The register block contains the following registers:

BITS	FUNCTION
D15:14	00 (index)
D13:0	Vector Diagonal Constant (K1)

TABLE 10-7. VECTOR DIAGONAL CONSTANT, BLOCK 7 INDEX 0

BITS	FUNCTION
D15:14	01 (index)
D13:0	Vector Orthogonal Constant (K2)

TABLE 10-8. VECTOR ORTHOGONAL CONSTANT, BLOCK 7 INDEX 1

BITS	FUNCTION
D15:14	10 (index)
D13:0	Vector Initial Error Constant (ET)

TABLE 10-9. VECTOR INITIAL ERROR CONSTANT, BLOCK 7 INDEX 2

10.9 CALCULATION OF VECTOR CONSTANTS

The constants required for generation of a vector are easily calculated by the host. These are based on the Bresenham algorithm.

For a vector from (x0,y0) to (x1,y1), first calculate:

$dx = |x1 - x0|$
$dy = |y1 - y0|$

Then calculate:

$dmin = \min(dx,dy)$
$dmax = \max(dx,dy)$

Finally calculate:

orthogonal constant = 2*dmin - 2*dmax
diagonal constant = 2*dmin
iec = 2*dim - dmax if $Xs \leq Xe$
or
iec = 2*dim - dmax -1 if $Xs > Xe$
Where iec = inital error constant

For fractional endpoints, the value of (x0,y0) and (x1,y1) may be multiplied by any constant to make all values integers.

11.0 SERIALIZER

11.1 OVERVIEW

The serializer controls how data is pixel interpreted in display memory and translated to the video output stream.

11.2 REGISTER MAP

INDEX	FUNCTION
0	Serial control
1	Serial row pitch
2	Serial start address low
3	Serial start address high
4	Serial memory mode
5	Reserved
6	Serial chromakey color low
7	Serial chromakey color high
8	Serial motion video window left
9	Serial motion video window right
A	Serial motion video window top
B	Serial motion video window bottom

NOTE:
The registers at index 1, 2, and 3 share certain bits with VGA CRTC registers and certain other bits of these registers can be automatically reset by writing the corresponding VGA registers

TABLE 11-1. SERIALIZER REGISTERS, BLOCK 11

11.3 SERIAL CONTROL REGISTER

The Serial Control register controls certain basic functions of the serializer.

BITS	FUNCTION
D15:12	0000 (index
D11:10	Not Used
D9	Serial YUV out code enable
D8	Serial YUV sync code enable
D7	Serial stretched YUV/Y enable
D6	Serial direct index enable
D5	Packed 24
D4	Serial YUV/Y conversion enable
D2:3	Serial motion video window enable
D1	Reserved
D0	Screen off

TABLE 11-2. SERIAL CONTROL, BLOCK 11 INDEX 0

D9	SERIAL YUV OUT CODE ENABLE (SHARE MODE ONLY)
1	Out Code Enable
0	Out Code Disable

NOTE:
Any YUV byte of 01 calls the next byte to exit from the motion video window.

D8	SERIAL YUV SYNC CODE ENABLE
1	Any YUV byte of 'FF' causes the next byte to be considered part of a new YUV group
0	Serial YUV sync codes are not enabled

D7	SERIAL YUV/Y STRETCHING ENABLE
1	YUV and Y stretching enabled*
0	YUV and Y stretching disabled

NOTE:
*This bit is useful only with YUV or Y formats.

D6	SERIAL DIRECT INDEX ENABLE
1	Direct indexed mode enabled*
0	Direct indexed mode disabled
NOTE: *This bit is useful only with YUV or Y formats.	

D5	PACKED 24
1	Enable Packed 24 (8/8) for Backup
0	Disable Packed 24

D4	SERIAL YUV/Y CONVERSION ENABLE
1	YUV to RGB conversion enable
0	YUV conversion disabled
NOTE: This bit is useful only with YUV or Y formats	

The YUV to RGB conversion is obtained through the CCIR 601 recommended formula as follows:

R = Y + 1.370 x (V - 128)
G = Y - 0.698 x (V - 128) - 0.336 X (V - 128)
B = Y + 1.730 x (V - 128)

D3	D2	SERIAL MOTION VIDEO WINDOW ENABLE
1	1	Display motion video window, force no occlusion
1	0	Reserved
0	1	Display motion video window
0	0	Do not display motion video window

D0	SCREEN OFF
1	Screen video is disabled (sync continues)
0	Screen video is enabled

11.4 START ADDRESS AND ROW PITCH

The Serial Start Address Low and High registers specify a 22-bit address in 32-bit doublewords of the memory location corresponding to the top-left corner of the screen. The Serial Row Pitch register specifies the offset in 64-bit chunks between the display locations containing vertical adjacent pixels.

This register is unaffected by scan doubling and the value in it ignores the zero-byte offset between vertically adjacent pixels of replicated lines.

BITS	FUNCTION
D15:12	0001 (index)
D11:0	Serial row pitch, in 64-bit chunks
NOTE: Bits 11:8 of this register are reset at power-up and may be reset by a write to the VGA Offset register, which may also write bits 7:0.	

TABLE 11-3. SERIAL ROW PITCH, BLOCK 11 INDEX 1

BITS	FUNCTION
D15:12	0010 (index)
D11:0	Serial start address bits 11:0, in 32-bit chunks
NOTE: Bit D11:0 must be a multiple of 64 bits in extended modes. These bits can be written by a write to the VGA Start Address register.	

TABLE 11-4. SERIAL START ADDRESS LOW, BLOCK 11 INDEX 2

BITS	FUNCTION
D15:12	0011 (index)
D11:8	Not Used
D7:0	Serial start address bits 19:12
NOTE: Bits 7:4 of this register are reset at power-up and may be reset by a write to either VGA Start Address register, which may also write bits 3:0	

TABLE 11-5. SERIAL START ADDRESS HIGH, BLOCK 11 INDEX 3

11.5 SERIAL MEMORY MODES

The Serial Memory Mode register specifies the format of pixels in display memory:

BITS	FUNCTION
D15:12	0100 (index)
D11:9	Serial motion video pixel format
D8:6	Serial motion video pixel size
D5	Serial desktop pixel format
D4:2	Serial desktop pixel size
D1:0	Serial memory sharing model
NOTE: Bits D4:0 are reset during power turn-on and reset	

TABLE 11-6. SERIAL MEMORY MODE, BLOCK 11 INDEX 4

D11	D10	D9	SERIAL MOTION VIDEO PIXEL FORMAT
1	1	0	Motion video window is Y color
1	0	1	Motion video window is YUV 4:1:1
1	0	0	Motion video window is YUV 4:2:2
0	1	0	Motion video window is direct color
0	0	0	Motion video window is indexed color
NOTE: Other values are reserved for future expansion			

D8	D7	D6	SERIAL MOTION VIDEO PIXEL SIZE
1	1	1	32 bits per pixel
1	1	0	Reserved
1	0	1	16 bits per pixel
1	0	0	15 bits per pixel
0	1	1	12 bits per pixel (YUV 4:1:1)
0	1	0	8 bits per pixel
0	0	1	Reserved
0	0	0	VGA compatibility format

D5	SERIAL DESKTOP PIXEL FORMAT
1	Desktop is direct color
0	Desktop is indexed color

D4	D3	D2	SERIAL DESKTOP PIXEL SIZE
1	1	1	32 bits per pixel
1	1	0	Reserved
1	0	1	16 bits per pixel
1	0	0	15 bits per pixel
0	1	1	Reserved
0	1	0	8 bits per pixel, II Mode if D5, D1, and D0 are all 0
0	0	1	4 bits per pixel
0	0	0	VGA compatibility format
NOTE: When Serial Desktop Pixel Size is set to 000, all other bits in this register are ignored and standard VGA register values are used.			

D1	D0	SERIAL MEMORY SHARING MODEL
1	1	Reserved
1	0	Desktop and inset window have shared memory
0	1	Desktop and inset window have separate memory
0	0	Desktop only, no inset window

11.6 BLOCK 11 INDEX 5 - RESERVED

11.7 DISPLAY LAYERS

For each location on the visible screen, a pixel is displayed from one of several sources. The pixel that is displayed on the screen is the composite of multiple "layers" of pixel data. In general, for each pixel, the non-transparent pixel on the highest active layer is displayed. When a layer is disabled, all pixels on that layer are transparent.

The lowest screen layer is the "overscan" layer and consists of the color specified in the Overscan Color register. When not disabled, pixels are displayed from this layer in the border region. When disabled, the screen in the border region is blanked. The next higher screen layer is the "desktop" layer, which corresponds to the basic display screen in a VGA or similar system. This layer is always enabled.

The next higher screen layer is "motion video window" layer. This layer is enabled whenever the Serial memory sharing model field of the Serial Memory Mode register is set to anything other than 00 and the Motion video window enable field in the Serial Control register is set to display the motion video window. Even when this layer is enabled, individual pixels from this layer may be transparent, depending on chromakey colors and the contents of the corresponding desktop layer pixel.

The highest screen layer is the "cursor" layer, which is described in the chapter on cursors. This layer differs slightly from the others in that it can modify (through inversion), rather than simply override, the data passed to it through the lower layers.

11.8 CHROMAKEY COLOR

The Serial Chromakey Color registers specify a chromakey color for desktop pixels when a motion video window is in use. These registers are used for desktop color modes using 8 and 16 bits per pixel.

BITS	FUNCTION
D15:12	0110 (index)
D11:8	Not Used
D7:0	Serial overlay color, bits 7:0
NOTE: The above register bits are also reset at power-on and reset.	

TABLE 11-7. SERIAL CHROMAKEY COLOR LOW, BLOCK 11 INDEX 6

BITS	FUNCTION
D15:12	0111 (index)
D11:8	Not Used
D7:0	Serial chromakey color, bits 15:8
NOTE: The above register bits are also reset at power-on and reset.	

TABLE 11-8. SERIAL CHROMAKEY COLOR HIGH BLOCK 11 INDEX 7

For 15-bit per pixel desktop modes, bit 15 of the desktop pixel is always used as the chromakey color. For 24-bit desktop modes, bit 31 is always used. In both cases, a '0' selects the desktop pixel and a '1' selects the motion video pixel.

11.9 MOTION VIDEO WINDOW

The four Serial Motion Video Window registers specify the location of the motion video window. The values inside these registers represent pixel locations, relative to the top-left corner of the visible screen. All of the pixel locations specified are inside the motion video window.

BITS	FUNCTION
D15:12	1000 (index)
D11:0	Serial motion video window, left boundary
NOTE: The above register bits are also reset at power-on and reset.	

TABLE 11-9. SERIAL MOTION VIDEO WINDOW LEFT, BLOCK 11 INDEX 8

BITS	FUNCTION
D15:12	1001 (index)
D11:0	Serial motion video window, right boundary
NOTE: The above register bits are also reset at power-on and reset.	

TABLE 11-10. SERIAL MOTION VIDEO WINDOW RIGHT, BLOCK 11 INDEX 9

BITS	FUNCTION
D15:12	1010 (index)
D11:0	Serial motion video window, top boundary
NOTE: The above register bits are also reset at power-on and reset.	

TABLE 11-11. SERIAL MOTION VIDEO WINDOW TOP, BLOCK 11 INDEX A

BITS	FUNCTION
D15:12	1011 (index)
D11:0	Serial motion video window, bottom boundary
NOTE: The above register bits are also reset at power-on and reset.	

TABLE 11-12. SERIAL MOTION VIDEO WINDOW BOTTOM, BLOCK 11 INDEX B

Outside of the motion video window, only desktop pixels are displayed. Within the motion video window, desktop or motion video pixels can be displayed, depending on the memory mode and chromakey colors.

11.10 DISPLAY OF MOTION VIDEO WINDOW PIXELS ON SCREEN

When no motion video window exists, all pixels are displayed from the desktop layer. Whenever a motion video window does exist, each pixel on the screen may be displayed from the desktop or motion video pixel data. (In the following discussion, the cursor layer is ignored.)

Outside of the motion video window, desktop layer pixels are always displayed.

Within an active motion video window, when a 'no occlusion' mode is selected, or when no occlusion is forced by the Serial Control register, motion video layer pixels are always displayed.

Otherwise, within an active motion video window, desktop or motion video pixel may be selected on a pixel-by-pixel basis, as follows:

In shared memory modes that permit occlusion, the high-order bit of the shared pixel is used to select the pixel for display. A '0' selects the desktop pixel and a '1' selects the motion video pixel. Note that in shared modes, all or part of the two pixels share physical memory. When the desktop and motion video pixels differ in size, the high-order bit of the larger pixel is used for selection.

In separate memory modes, the desktop pixel determines which pixel is displayed. In some cases, the desktop pixel is compared to a chromakey color, and matching pixels cause the motion video pixel to be displayed. In other cases, the high-order bit of the desktop pixel is used, with a '0' selecting the desktop pixel and a '1' selecting the motion video pixel.

11.11 VGA CRTC REGISTER LOCKING FOR SERIALIZER REGISTERS

If the Lock VGA CRT Controller registers bit is set in the VGA Lock Control register, then all VGA CRTC registers are locked and cannot be written through the VGA ports.

However, if this bit is not set, then writes to any of the following VGA registers immediately cause the following extended register bits to be reset to 0:

REGISTER	FUNCTION
3?5h.13h	Serial row pitch, bits 11:8
3?5h.0Dh	Serial start address high, bits 7:4
3?5h.0Ch	Serial start address high, bits 7:4

NOTE:
(3) Writing to a register resets the serializer bits.
(4) The above register bits are also reset at power-on and reset.

TABLE 11-13. SERIALIZER REGISTER AUTO-RESET

12.0 STRETCH REGISTERS

Stretch (scaling and interpolation) registers control motion video data in stretch mode. In this mode, the horizontal and vertical directions have different scaling factors, which are specified by registers in index 2 and 3, respectively. These registers only support stretch mode when the destination pixel/line count is greater than or equal to the source pixel/line count. These registers do not support shrinking when the destination pixel/line count is less than the source pixel/line count.

12.1 REGISTER MAP

The register map is shown in Table 12-1.

INDEX	FUNCTION
0	Motion Video Source Data Start Address Low
1	Motion Video Source Data Start Address High
2	Horizontal Scaling Factor
3	Vertical Scaling Factor
4	Motion Video Source Data Line Offset
5	Motion Video Source Data Line Width

TABLE 12-1 STRETCH REGISTER, BLOCK 9

12.2 START ADDRESS

The Motion Video Source Data Start Address Low and High registers specify a 20-bit address in 64-bit (two double words) boundary of the memory location corresponding to the top left corner of the screen. The Motion Video Source Data Line Offset register specifies the offset in 64-bit segments between the source data locations containing adjacent vertical pixels.

BITS	FUNCTION
D15:12	0000 (index)
D11:0	Motion Video Source Data Start Address Bits 11:0, in 64-bit segments

TABLE 12-2. MOTION VIDEO SOURCE DATA START ADDRESS LOW, BLOCK 9, INDEX 0

BITS	FUNCTION
D15:12	0001 (index)
D11:8	Reserved
D7:0	Motion Video Source Data Start Address Bits 19:12, in 64-bit segments

TABLE 12-3. MOTION VIDEO SOURCE DATA START ADDRESS HIGH, BLOCK 9, INDEX 1

BITS	FUNCTION
D15:12	0100 (index)
D11:0	Motion Video Source Data Line Offset, in 64-bit segments

TABLE 12-4. MOTION VIDEO SOURCE DATA LINE OFFSET, BLOCK 9, INDEX 4

12.3 SCALING FACTOR

The Horizontal and Vertical Scaling Factor registers specify the horizontal and vertical directions, respectively. The following equation is used to calculate the scaling factor in either direction.

Scaling Factor = 4096d/Destination or Source

Where: 4096 is in decimal notation and the 12 least significant bits (LSB) of the result are loaded into the registers.

BITS	FUNCTION
D15:12	0010 (index)
D11:0	Horizontal Scaling Factor

TABLE 12-5. HORIZONTAL SCALING FACTOR, BLOCK 9, INDEX 2

BITS	FUNCTION
D15:12	0010 (index)
D11:0	Vertical Scaling Factor

TABLE 12-6. VERTICAL SCALING FACTOR, BLOCK 9, INDEX 3

12.4 SOURCE DATA LINE WIDTH

The Motion Video Source Data Line Width register specifies the number of pixels per line minus one.

BITS	FUNCTION
D15:12	0010 (index)
D11:0	Motion Video Source Data Line Width

TABLE 12-7. MOTION VIDEO SOURCE DATA LINE WIDTH, BLOCK 9, INDEX 5

13.0 DIRECT INDEXED COLOR REGISTERS

13.1 OVERVIEW

The Direct Indexed Color Registers block supports a special 8-bit direct-indexed color mode in which an 8-bit RGB (3-3-2) color mode is "color corrected" to permit more precise control of the red, green, and blue intensities. Rather than directly supplying a 2- or 3-bit color intensity, each of the 2 and 3 bit color values indexes an independent palette which provides a 6-bit intensity.

13.2 REGISTER MAP

The direct-indexed color registers are available through the extended register address space. These registers are overlaid with the VGA Attribute Controller register block.

INDEX	FUNCTION
00	Direct Indexed Red Color 0
⇓	⇓
07	Direct Indexed Red Color 7
08	Direct Indexed Green Color 0
⇓	⇓
0F	Direct Indexed Green Color 7
10	Direct Indexed Blue Color 0
11	Overscan Color (refer to note)
12	Direct Indexed Blue Color 1
13	Direct Indexed Blue Color 2
14	Direct Indexed Blue Color 3

NOTE:
Index 11 is the same register found in the VGA Attribute Controller register block.

TABLE 13-1. DIRECT INDEXED COLOR REGISTERS - OVERLAID WITH ATTRIBUTE CONTROLLER REGISTERS (BLOCK 30)

NOTE

The Overscan Color register has been left in its Attribute Controller index location and other registers skipped over it.

13.3 COLOR REGISTERS

There are 20 color registers, each with the same format. One example is shown here.

BITS	FUNCTION
D15:8	0000 0000 (index)
D7:6	Not Used
D5:0	Red component for red index 0

TABLE 13-2. DIRECT INDEXED RED COLOR 0, BLOCK 30 INDEX 0

13.4 DISPLAY OF DIRECT-INDEXED VALUES

When 8-bit direct color mode is selected for display, then each 8-bit pixel contains red, green, and blue components as follows:

BITS	FUNCTION
D7:5	Red component
D4:2	Green component
D1:0	Blue component

TABLE 13-3. DIRECT COLOR PIXEL FORMAT

When the Serial Direct Index Enable bit is not set in the Serial Control register, these components directly specify the red, green, and blue intensity values for the current pixel. Each field represents the 2 or 3 most significant bits of the respective color value.

When this bit is set, however, each of the above fields selects one of four or eight 6-bit intensity values for its respective color from the 20 intensity values in the Direct Indexed Color register block. Note that each field can affect only the intensity of its own color component. The 6-bit intensities represent the a 6-bit fraction of full-scale color, and are automatically adjusted to 5-bit or 8-bit DACs by low-order truncation or zero padding as required.

14.0 CLOCK GENERATOR

14.1 OVERVIEW

The internal dual-clock generator provides separate clock frequencies for the video dot clock (VCLK) and the memory clock (MCLK). Also, external sources can be used to generator either or both clocks. An external clock generator can be attached to data lines MD7:0 when the WCLK pin is used to strobe data into the external clock generator.

14.2 REGISTER MAP

INDEX	FUNCTION
0	VCLK Generator Control
1	VCLK Programmable Frequency
2	MCLK Generator Control
3	MCLK Programmable Frequency
4	TRLCK/PCLK Generator Control
5	CLOCK Programmable Skew

TABLE 14-1. CLOCK GENERATOR REGISTERS, BLOCK 17

14.3 VCLK GENERATOR REGISTERS

The VCLK clock generator registers control the internal VCLK generator circuits.

BITS	FUNCTION
D15:12	0000 (index)
D11	VCLK lock 3C2h clock select bit
D10	VCLK external clock load enable
D9:8	Reserved
D7:6	VCLK frequency select
D5:3	Reserved
D2	VCLK generator state
D1	VCLK Equal
D0	VCLK source

NOTE:

(1) Bits D10, D2, and D0 share configuration pin CNF00.

(2) Bits D1 and D11 are reset at power turn-on and reset.

(3) Bits D7:6 are reset to 00 at power turn-on and reset.

TABLE 14-2. VCLK GENERATOR CONTROL BLOCK 17 INDEX 0

D11	LOCK 3C2h CLOCK SELECT BITS
1	Writes to 3C2h do not set clock frequency fields
0	Writes to 3C2h set VCLK frequency fields

D10	EXTERNAL VCLK LOAD ENABLE
1	Strobe WCLK on changes to VCLK frequencies(2)
0	Do not strobe WCLK on changes to VCLK frequencies(1)

NOTE:

(1) This is the power-on setting when the VCLK Source configuration bit is high on reset

(2) This is the power-on setting when the VCLK Source configuration bit is low on reset

D7:6	VCLK FREQUENCY SELECT

NOTE:
Bits D7:6 select VSEL1:0, respectively. Refer to Table 14-3. These bits are set to 00 at power-on and reset.

D2	VCLK GENERATOR STATE
1	VCLK generator is operational(1)
0	VCLK generator is off(2)

NOTE:

(1) This is the power-on setting when the VCLK Source configuration bit is high on reset

(2) This is the power-on setting when the VCLK Source configuration bit is low on reset

D1	VCLK EQUAL
1	VCLK is the same as MCLK
0	VCLK is different from MCLK

D0	VCLK SOURCE
1	VCLK source is internal clock generator(1)
0	VCLK source is VCLK input pin(2)

NOTE:
(1) This is the power-on setting when the VCLK Source configuration bit is high on reset
(2) This is the power-on setting when the VCLK Source configuration bit is low on reset

NOTE:

VSEL1:0 (Block 17 Index 0, bits D7:6) are used to select the internal VCLK frequency as listed in Table 14-3. VSEL3:2 (Port 3C2h/3CCh, bits 3:2) are used to select the Video Clock.

VSEL 1	VSEL 0	TARGET FREQUENCY (MHz)	ACTUAL FREQUENCY (MHz)
0	0	25.175000	25.172284
0	1	28.322000	28.325095
1	0	Programmable Frequency	(14.31818/32) * N N is from Table 14-4, bits D8:0
1	1		

NOTE:
In the programmable frequency mode for VCLK, frequencies in the range of 25.057 MHz to 135.128 MHz can be generated in 447.443 KHz increments. The N value is used to calculate the programmable frequency as follows:

$$f = (14.31818\ MHz/32) \times N$$

Where f is the programmable frequency in MHz.

TABLE 14-3. VCLK FREQUENCY SELECTION

The VCLK Programmable Frequency register (Table 14-4) specifies the frequency to be generated for VCLK when the programmable frequency mode is selected by the VCLK Frequency Select register (Table 14-2, bits D7:6).

The programmable frequency is selected in terms of the VCLK input frequency, which is assumed to be 14.31818 MHz (refer to Table 14-3).

BITS	FUNCTION
D15:12	0001 (index)
D11:9	Not Used
D8:0	VCLK programmable frequency

TABLE 14-4. VCLK PROGRAMMABLE FREQUENCY, BLOCK 17 INDEX 1

14.4 MCLK GENERATOR REGISTERS

The MCLK clock generator registers control the internal MCLK generator circuits.

BITS	FUNCTION
D15:12	0010 (index)
D11:7	Not Used
D6:4	MCLK frequency select
D3	Reserved
D2	MCLK generator state
D1	Reserved
D0	MCLK source

NOTE:
(1) Bits D0 and D2 share configuration pin CNF01.
(2) Bits D6:4 are configuration bits CNF04:02.

TABLE 14-5. MCLK GENERATOR CONTROL, BLOCK 17 INDEX 2

D6:4	MCLK FREQUENCY SELECT

NOTE:
(1) Bits D6:4 select MSEL2:0, respectively. These bits are set by configuration bits during power-on and reset to select the MCLK frequency.
(2) Bits D6:4 are also used by the BIOS to set the MCLK Programmable Frequency, Block 17 Index 3 register. At power-on or reset, the register (MN7:0) is set to 6Eh, which generates a 49.218 MHz MCLK frequency.

D2	MCLK GENERATOR STATE
1	MCLK generator is operational
0	MCLK generator is off(2)

NOTE:
(1) This is the power-on setting when the MCLK Source configuration bit is high on reset
(2) This is the power-on setting when the MCLK Source configuration bit is low on reset

D0	MCLK SOURCE
1	MCLK source is internal clock generator(1)
0	MCLK source is MCLK input pin(2)

NOTE:
(1) This is the power-on setting when the MCLK Source configuration bit is high on reset
(2) This is the power-on setting when the MCLK Source configuration bit is low on reset

For MCLK, frequencies in the range of 44.744 MHz to 85.014 MHz can be generated in 447.443 KHz increments. The N value is used to calculate the programmable frequency as follows:

$$f = (14.31818\ MHz/32) * N$$

Where f is the programmable frequency in MHz.

The MCLK Programmable Frequency register (Table 14-6) specifies the frequency to be generated for MCLK.

The programmable frequency is selected in terms of the MCLK input frequency, which is assumed to be 14.31818 MHz.

BITS	FUNCTION
D15:12	0011 (index)
D11:8	Not Used
D7:0	MCLK programmable frequency

TABLE 14-6. MCLK PROGRAMMABLE FREQUENCY, BLOCK 17 INDEX 3

14.5 COMPATIBILITY WITH VGA

When the External VCLK Load Enable bit is set, a change to the 4-bit VCLK Frequency field in the VCLK Generator Control register causes a register load cycle to occur. The new contents of the field affect the external clock generator.

When the Lock Port 3C2h bit is not set, a write to port 3C2h also causes the VCLK External and Internal Frequency fields to be modified. If the VCLK External Clock Load Enable bit is set in the VCLK Generator Control register, a register load cycle occurs automatically, and affects the clock generator based on the new contents of this register. When the Lock Port 3C2h bit is set, a write to 3C2h has no effect on the VCLK Frequency field and no register load cycle occurs.

With the lock bit not set, a write to port 3C2h updates to the VCLK External and Internal Frequency fields as listed in Table 14-8.

3C2h		INTERNAL FREQUENCY	EXTERNAL FREQUENCY
D3	D2		
1	1	0011 (80.000 MHz)	11
1	0	0010 (programmable frequency)	10
0	1	1101 (28.325 MHz)	01
0	0	1100 (25.175 MHz)	00

TABLE 14-7. VGA PORT 3C2h TO VCLK FREQUENCY MAPPING

14.6 TRCLK/PCLK GENERATOR CONTROL

BITS	FUNCTION
D15:12	0100 (index)
D11:4	Not Used
D3	PCLK State
D2	PCLK Phase
D1	VAFC PCLK Out
D0	Transfer Clock (TRCLK) Source
NOTE: TRCLK is the internal video transfer clock at the video pipeline.	

TABLE 14-8. TRCLK/PCLK GENERATOR REGISTER, BLOCK 17 INDEX 4

D3	PCLK STATE
1	PCLK Off(2)
0	PCLK On(1)

NOTES:
(1) This is the power-on setting when the Internal RAMDAC (CNF6) and VAFC Disable (CNF33) configuration bits are both high at power-on or reset. Refer to Section 25.4, *Configuration Options.*
(2) This is the power-on setting when the Internal RAMDAC (CNF6) bit or VAFC Disable (CNF33) bit is low at power-on or reset.

D2	PCLK PHASE
1	PCLK to Output Pin is the Same Phase as PCLK to VGA Core
0	PCLK to Output Pin is the Inversion of PCLK to VGA Core
NOTE: This bit is reset at power-on and reset.	

D1	VAFC PCLK OUT
1	PCLK is VCLK Divided by 2
0	PCLK is VCLK
NOTE: This bit is set to 1 at power-on and reset.	

D0	TRANSFER CLOCK (TRCLK) SOURCE
1	TRCLK is VCLK Divided by 2
0	TRCLK is VCLK
NOTE: This bit is set to 1 at power-on and reset.	

14.7 CLOCK PROGRAMMABLE SKEW

BITS	FUNCTION
D15:12	0101 (index)
D11:8	Not Used
D7:4	MCLK to MDCLK Skew
D3:0	TRCLK to VCLK Skew

NOTE:
Bits 7:0 are set at power-on by configuration bits as follows:
D7 = CNF46
D6 = CNF45
D5 = CNF44
D4 = CNF43
D3 = CNF39
D2 = CNF38
D1 = CNF37
D0 = CNF36

TABLE 14-9. CLOCK PROGRAMMABLE SKEW REGISTER, BLOCK 17 INDEX 5

15.0 CRT CONTROLLER

15.1 OVERVIEW

The CRT controller registers define the horizontal and vertical timing of the WD9710. They also control certain screen display, scrolling, panning, text, and block cursor parameters.

All VGA CRTC registers may be accessed in three different ways.

These registers may be accessed through the standard VGA 3B4/3B5 and 3D4/3D5 ports in the normal manner.

Additionally, these same registers may be accessed through the 8-bit VGA CRT Controller register block.

Finally, some of these registers may be accessed through the 12-bit Extended CRT Controller register block, which permits unbroken access to many fields split between registers in standard VGA, and others may be accessed through the 12-bit Serializer register block.

15.2 VGA REGISTER ACCESS MAP

The VGA registers are accessed through ports 3?4h and 3?5h as follows:

Port 3?4h CRT Controller Index
Port 3?5h CRT Controller Data

The ? refers to Bh or Dh depending on the value of the I/O Address Select bit of the Miscellaneous Output register (port 3C2h). In addition to the indexed locations listed in Table 15-1, VGA CRTC registers can be accessed as 8-bit registers through the VGA CRT Controller register block. Other ways to access some these registers are indicated in the same table.

INDEX	FUNCTION
00	Horizontal Total(1)
01	Horizontal Display Enable End(1)
02	Horizontal Blank Start(1)
03	Horizontal Blank End(1)
04	Horizontal Sync Start(1)
05	Horizontal Sync End(1)
06	Vertical Total(1)
07	Overflow(1)
08	Preset Row Scan
09	Maximum Scan Line
0A	Block Cursor Start
0B	Block Cursor End
0C	Start Address High(2)
0D	Start Address Low(2)
0E	Block Cursor Location High
0F	Block Cursor Location Low
10	Vertical Sync Start(1)
11	Vertical Sync End(1)
12	Vertical Display Enable End(1)
13	Offset(2)
14	Underline Location
15	Vertical Blank Start(1)
16	Vertical Blank End(1)
17	CRTC Mode Control
18	Line Compare(1)

NOTE:
(1) The bits in these registers can be accessed in a different order through the 12-bit Extended CRT Controller register block
(2) These registers can be accessed through the 12-bit Serializer register block

TABLE 15-1. CRTC REGISTERS (VGA ACCESS), PORT 3?4h/3?5h

15.3 CRT CONTROLLER INDEX REGISTER

BITS	FUNCTION
D7:5	Not Used
D4:0	Index
NOTE: Bits D4:0 are reset at power-on and reset.	

TABLE 15-2. CRTC INDEX (VGA ACCESS ONLY), PORT 3?4

15.4 HORIZONTAL TIMING REGISTERS

The Horizontal Total register defines the horizontal period, in character clocks, less five. The Horizontal Display Enable registers specifies the width of the active region, in character clocks, less one.

BITS	FUNCTION
D7:0	Horizontal total period, less 5 (in character clocks)
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-3. HORIZONTAL TOTAL, PORT 3?5 INDEX 0

BITS	FUNCTION
D7:0	Number of displayed characters, less 1
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-4. HORIZONTAL DISPLAY ENABLE END, PORT 3?5 INDEX 1

The Horizontal Blank Start register defines the number of character clocks from the start of line where horizontal blanking is asserted, less one. The Horizontal Blank End register defines the location within the line where horizontal blanking is de-asserted. Note that the Horizontal Blank End field is smaller than the horizontal counter, and horizontal blanking is de-asserted when the 6 bits of the field match the 6 low-order bits of the horizontal counter. Note also that the horizontal blanking pulse can straddle the start of line.

BITS	FUNCTION
D7:0	Horizontal Blank Start
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-5. HORIZONTAL BLANK START, PORT 3?5 INDEX 2

BITS	FUNCTION
D7	Not Used
D6:5	Display Enable Skew, in character clocks
D4:0	Horizontal Blank End, bits 4:0(2)
NOTE: (1) Bits 6:0 are reset at power-on and reset. (2) The remainder of this field is located at index 5, bit 7	

TABLE 15-6. HORIZONTAL BLANK END, PORT 3?5 INDEX 3

The Horizontal Sync Start register defines the number of character clocks from the start of line where horizontal sync is asserted. The Horizontal Sync End register defines the location within the line where horizontal sync is de-asserted. Note that the Horizontal Sync End field is smaller than the horizontal counter, and horizontal sync is de-asserted when the field match the 5 low-order bits of the horizontal counter. Note also that the horizontal sync pulse can straddle the start of line.

BITS	FUNCTION
D7:0	Horizontal Sync Start
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-7. HORIZONTAL SYNC START, PORT 3?5 INDEX 4

BITS	FUNCTION
D7	Horizontal blank end, bit 6(2)
D6:5	Horizontal sync Skew, in character clocks
D4:0	Horizontal sync end

NOTE:
(1) Bits D7:0 are reset at power-on and reset.
(2) The remainder of this field is located at index 3, bits D4:0.

TABLE 15-8. HORIZONTAL SYNC END, PORT 3?5 INDEX 5

15.5 VERTICAL TIMING REGISTERS

The Vertical Total register defines the vertical period, in character clocks, less five. The Vertical Display Enable register specifies the height of the active region, in character clocks, less one.

BITS	FUNCTION
D7:0	Vertical total period, less 2 (in scan lines

NOTE:
Bits D7:0 are reset at power-on and reset.

TABLE 15-9. VERTICAL TOTAL, PORT 3?5 INDEX 6

BITS	FUNCTION
D7:0	Vertical display enable end, less 1, bits 7:0

NOTE:
The remainder of this field is located at index 7, bits D6 and D1.

TABLE 15-10. VERTICAL DISPLAY ENABLE END, PORT 3?5 INDEX 12

The Vertical Blank Start and Vertical Blank End registers define the locations within the screen where vertical blanking is active. These registers are analogous to the Horizontal Blank Start and End registers. Note, however, that the register values are in scan lines and the Vertical Blank End register is 8 bits and does not contain additional fields.

BITS	FUNCTION
D7:0	Vertical blank start, less 1, bits 7:0(2)

NOTE:
(1) Bits D7:0 are reset at power-on and reset.
(2) The remainder of this field is located at index 7, bit D3 and at index 9, bit D5.

TABLE 15-11. VERTICAL BLANK START, PORT 3?5 INDEX 15

BITS	FUNCTION
D7:0	Vertical blank end, less 1

NOTE:
Bits D7:0 are reset at power-on and reset.

TABLE 15-12. VERTICAL BLANK END, PORT 3?5 INDEX 16

The Vertical Sync Start and Vertical Sync End registers define the locations within the screen where vertical sync is active. These registers are analogous to the Horizontal Sync Start and End registers. Note, however, that the register values are in scan lines and that the Vertical Sync End field is 4 bits.

BITS	FUNCTION
D7:0	Vertical sync start, bits 7:0(2)

NOTE:
(1) Bits D7:0 are reset at power-on and reset.
(2) The remainder of this field is located at index 7, bits D9:8.

TABLE 15-13. VERTICAL SYNC START, PORT 3?5 INDEX 10

BITS	FUNCTION
D7	CRTC 0-7 write protect
D6	DRAM refresh control
D5	Vertical interrupt enable
D4	Vertical interrupt clear
D3:0	Vertical sync end
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-14. VERTICAL SYNC END, PORT 3?5 INDEX 11

D7	CRTC 0-7 write protect
1	CRTC registers 0-7 are locked, except *Vertical Overflow* register bit 4*
0	CRTC registers 0-7 can be written
NOTE: In either case, this bit can still be written through either CRTC Extended register block	

D6	DRAM REFRESH CONTROL
1	Generate five refresh cycles per scan line
0	Generate three refresh cycles per scan line

D5	VERTICAL INTERRUPT ENABLE
1	Disable vertical retrace interrupt
0	Enable vertical retrace interrupt

D4	VERTICAL INTERRUPT CLEAR
1	Clear vertical interrupt
0	Vertical interrupt may be permitted
NOTE: This bit is pulsed high to clear a vertical interrupt	

The Line Compare register specifies a vertical counter value where the video refresh address counter is cleared. This may be used for split screen operation.

BITS	FUNCTION
D7:0	Line compare, bits 7:0(1)
NOTE: (1) Bits D7:0 are reset at power-on and reset. (2) The remainder of this field is located at index 7, bit D4 and index 9, bit 6.	

TABLE 15-15. LINE COMPARE, PORT 3?5 INDEX 18

The Vertical Overflow counter contains high-order bits for certain vertical timing registers. A few other high-order bits are contained in the Maximum Scan Line register.

When writing the CRT controller using extended registers, these overflow register bits do not exist, rather, they are appended to the register values being written.

BITS	FUNCTION
D7,2	Vertical sync start, bits 9:8
D5,0	Vertical total, bits 9:8
D6,1	Vertical display enable end, bits 9:8
D4	Line compare, bit 9
D3	Vertical blank start, bit 8
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-16. VERTICAL OVERFLOW, PORT 3?5 INDEX 7

15.6 TEXT MODE REGISTERS

The Preset Row Scan register permits smooth panning and scrolling of text. The Preset Row Scan field specifies which line of the first character row appears at the top of the screen. The Byte Panning Control selects a number of bytes, from 0 to 3, by which to pan the entire screen to the left.

BITS	FUNCTION
D7	Not Used
D6:5	Byte panning control
D4:0	Preset row scan
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-17. PRESET ROW SCAN, PORT 3?5 INDEX 8

BITS	FUNCTION
D7	Double scanning enable
D6	Line compare, bit 9
D5	Vertical blank start, bit 9
D4:0	Number of scan lines per character row, less 1
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-18. MAXIMUM SCAN LINE, PORT 3?5 INDEX 9

15.7 BLOCK CURSOR REGISTERS

The Block Cursor Start Line field specifies the scan line number within a character block where the block cursor begins, less 1. The Block Cursor End Line field specifies the ending scan line number.

BITS	FUNCTION
D7:6	Not Used
D5	Block cursor control
D4:0	Block cursor start line, less 1
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-19. BLOCK CURSOR START, PORT 3?5 INDEX A

D5	BLOCK CURSOR CONTROL
1	Block cursor off
0	Block cursor on

BITS	FUNCTION
D7	Not Used
D6:5	Block cursor skew, in character clocks
D4:0	Block cursor end line
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-20. BLOCK CURSOR END, PORT 3?5 INDEX B

The Block Cursor Location High and Low registers specify the character location in display memory of the character where the block cursor appears.

NOTE

The registers point to the character in display memory, not to a location on the screen.

BITS	FUNCTION
D7:0	Block cursor location, bits 15:8(2)
NOTE: (1) Bits D7:0 are reset at power-on and reset. (2) The remainder of this field is located at index F, bits D7:0	

TABLE 15-21. BLOCK CURSOR LOCATION HIGH, PORT 3?5 INDEX E

BITS	FUNCTION
D7:0	Block cursor location, bits 7:0(2)
NOTE: (1) Bits D7:0 are reset at power-on and reset. (2) The remainder of this field is located at index E, bits D7:0	

TABLE 15-22. BLOCK CURSOR LOCATION LOW, PORT 3?5 INDEX F

The Underline Location field specifies the scan line number, within each character row, where underlining, if specified for a given character, takes place.

BITS	FUNCTION
D7	Not Used
D6	Doubleword mode ***VGA bit not supported***
D5	Count by 4 ***VGA not supported***
D4:0	Underline
NOTE: Bits D6:0 are reset at power-on and reset.	

TABLE 15-23. UNDERLINE LOCATION, PORT 3?5h INDEX 14h

D6	DOUBLEWORD MODE
1	Doubleword addressing
0	Normal

D5	COUNT BY 4
1	Divide clock to memory address counted by 4
0	Normal

15.8 VIDEO REFRESH REGISTERS

The Start Address High and Low registers specify the location in display memory, in doublewords. corresponding to the top-left corner of the visible screen. The Offset register specifies the row pitch, in words or doublewords, between scan lines in display memory.

Writing any of these register may also set reset certain high-order bits in the corresponding extended registers.

BITS	FUNCTION
D7:0	Start address, bits 15:8(2)
NOTE: (1) Bits D7:0 are reset at power-on and reset. (2) The remainder of this field is located at index D, bits D7:0	

TABLE 15-24. START ADDRESS HIGH, PORT 3?5 INDEX C

BITS	FUNCTION
D7:0	Start address, bits 7:0(2)
NOTE: (1) Bits D7:0 are reset at power-on and reset. (2) The remainder of this field is located at index C, bits D7:0	

TABLE 15-25. START ADDRESS LOW, PORT 3?5h INDEX Dh

BITS	FUNCTION
D7:0	Screen row pitch(2)
NOTE: (1) Bits D7:0 are reset at power-on and reset. (2) The value is given in physical doublewords	

TABLE 15-26. OFFSET PORT 3?5h INDEX 13h

15.9 CRTC MODE REGISTER

BITS	FUNCTION
D7	Hardware reset
D6	Word or byte mode
D5	Address wrap
D4	Not Used
D3	Count by 2 ***VGA bit not supported***
D2	Horizontal retrace select ***VGA not supported***
D1:0	CGA compatibility ***VGA not fully supported***
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-27. CRTC MODE CONTROL, PORT 3?5 INDEX 17

D7	HARDWARE RESET
1	Normal
0	Reset retrace signals

D6	WORD OR BYTE MODE
1	Byte mode
0	Word mode

NOTE:
This bit is irrelevant if the Doubleword Mode bit in the Underline Location register (index 14) is set.

D5	ADDRESS WRAP
1	The full addressing range is available
0	Addresses wrap into 64K bytes

D3	COUNT BY 2 ***VGA NOT SUPPORTED***
1	Divide clock to memory address counter by 2
0	Normal

D2	HORIZONTAL RETRACE SELECT ***VGA NOT SUPPORTED***
1	Clock vertical counter with one-half horizontal timing
0	Normal

D1	D0	CGA COMPATIBILITY
1	1	Scan lines are contiguous
1	0	Scan lines are 8K bytes apart
0	1	Scan lines are 16K bytes apart ***VGA not** supported***
0	0	(not used in VGA) ***VGA not supported***

NOTE:
Bits D6:0 are reset at power-on and reset.

15.10 REGISTER MAP (EXTENDED ACCESS)

INDEX	FUNCTION
0	Horizontal Interlaced Offset(1)
1	Horizontal Total(2)
2	Horizontal Display Enable End(2)
3	Horizontal Blank Start(2)
4	Horizontal Blank End
5	Horizontal Sync Start(2)
6	Horizontal Sync End
7	CRTC Miscellaneous
8	Vertical Total(2)
9	Vertical Active(2)
A	Vertical Blank Start (2)
B	Vertical Blank End
C	Vertical Sync Start(2)
D	Vertical Sync End
E	Line Compare(2)

NOTES:
(1) This is not a standard VGA CRTC register.
(2) Bits that are not included in VGA registers are reset at power-on and rest.

TABLE 15-28. CRTC REGISTERS (EXTENDED ACCESS), BLOCK 15

15.11 HORIZONTAL TIMING REGISTERS (EXTENDED ACCESS)

The following registers are an alternate way to access the VGA CRTC horizontal timing registers. Generally, fields split between registers have been gathered together, and most registers have been extended in length.

The Horizontal Interlace Offset register is not a standard VGA register. It specifies the one-half scan line offset to be used for the VSYNC signal between fields of a frame.

BITS	FUNCTION
D15:12	0000 (index)
D11:8	Not Used
D7:0	Horizontal interlace offset (in character clocks)
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-29. HORIZONTAL INTERLACE OFFSET, BLOCK 15 INDEX 0

BITS	FUNCTION
D15:12	0001 (index)
D11:9	Not Used
D8:0	Horizontal total period, less 5 (in character clocks)
NOTE: Bits D8:0 are reset at power-on and reset.	

TABLE 15-30. HORIZONTAL TOTAL, BLOCK 15 INDEX 1

BITS	FUNCTION
D15:12	0010 (index)
D11:9	Not Used
D8:0	Horizontal active region, less 1 (in character clocks)
NOTE: Bits D8:0 are reset at power-on and reset.	

TABLE 15-31. HORIZONTAL DISPLAY ENABLE END, BLOCK 15 INDEX 2

BITS	FUNCTION
D15:12	0011 (index)
D11:9	Not Used
D8:0	Horizontal blank start (in character clocks)
NOTE: Bits D8:0 are reset at power-on and reset.	

TABLE 15-32. HORIZONTAL BLANK START, BLOCK 15 INDEX 3

BITS	FUNCTION
D15:12	0100 (index)
D11:6	Not Used
D5:0	Horizontal blank end (in character clocks)
NOTE: Bits D5:0 are reset at power-on and reset.	

TABLE 15-33. HORIZONTAL BLANK END, BLOCK 15 INDEX 4

BITS	FUNCTION
D15:12	0101 (index)
D11:9	Not Used
D8:0	Horizontal sync start (in character clocks)
NOTE: Bits D8:0 are reset at power-on and reset.	

TABLE 15-34. HORIZONTAL SYNC START, BLOCK 15 INDEX 5

BITS	FUNCTION
D15:12	0110 (index)
D11:5	Not Used
D4:0	Horizontal sync end (in character clocks)
NOTE: Bits D4:0 are reset at power-on and reset.	

TABLE 15-35. HORIZONTAL SYNC END BLOCK 15 INDEX 6

15.12 CRTC MISCELLANEOUS REGISTER

The CRTC Miscellaneous register contains the various standard VGA register bits contained in the CRTC registers covered by this section but not included in extended registers themselves.

BITS	FUNCTION
D15:12	0111 (index)
D11:8	Not Used
D7	CRTC 0-7 write protect
D6	Select 3/5 DRAM refresh
D5	Enable vertical interrupt
D4	Clear vertical interrupt
D3:2	Horizontal sync skew
D1:0	Display enable skew
NOTE: Bits D15:0 are reset at power-on and reset.	

TABLE 15-36. CRTC MISCELLANEOUS, BLOCK 15 INDEX 7

15.13 VERTICAL TIMING REGISTERS (EXTENDED ACCESS)

The following registers are an alternate way to access the VGA CRTC vertical timing registers. Generally, fields split between registers have been gathered together, and most registers have been extended in length.

BITS	FUNCTION
D15:12	1000 (index)
D11:0	Vertical total period less 2 (in scan lines)
NOTE: Bits D11:0 are reset at power-on and reset.	

TABLE 15-37. VERTICAL TOTAL, BLOCK 15 INDEX 8

BITS	FUNCTION
D15:12	1001 (index)
D11:0	Vertical active region, less 1
NOTE: Bits D11:0 are reset at power-on and reset.	

TABLE 15-38. VERTICAL DISPLAY ENABLE END, BLOCK 15 INDEX 9

BITS	FUNCTION
D15:12	1010 (index)
D11:0	Vertical blank start
NOTE: Bits D11:0 are reset at power-on and reset.	

TABLE 15-39. VERTICAL BLANK START, BLOCK 15 INDEX A

BITS	FUNCTION
D15:12	1011 (index)
D11:8	Not Used
D7:0	Vertical blank end
NOTE: Bits D7:0 are reset at power-on and reset.	

TABLE 15-40. VERTICAL BLANK END, BLOCK 15 INDEX B

BITS	FUNCTION
D15:12	1100 (index)
D11:0	Vertical sync start
NOTE: Bits D11:0 are reset at power-on and reset.	

TABLE 15-41. VERTICAL SYNC START, BLOCK 15 INDEX C

BITS	FUNCTION
D15:12	1101 (index)
D11:4	Not Used
D3:0	Vertical sync end
NOTE: Bits D3:0 are reset at power-on and reset.	

TABLE 15-42. VERTICAL SYNC END, BLOCK 15 INDEX D

BITS	FUNCTION
D15:12	1110 (index)
D11:0	Line compare
NOTE: Bits D11:0 are reset at power-on and reset.	

TABLE 15-43. LINE COMPARE, BLOCK 15 INDEX E

15.14 CRTC REGISTER ACCESS

All CRTC registers are always writable through either the Extended CRTC Registers or the VGA CRTC Registers register blocks. Writes through the VGA CRTC port (3?4/5) are subject to locking.

If the Lock VGA CRTC Controller Register bit is set in the VGA Lock Control register, then VGA CRTC registers 00-07h, 09h bits 6:5, 10-12h, 15-16h, and 18h are locked and cannot be written through the VGA ports.

However, if the CRTC Lock bit is not set, then writes to any of the following VGA registers immediately cause the corresponding extended register bits to be reset to 0:

VGA REGISTER INDEX	EXTENDED REGISTER BITS RESET
0	Index 1, Horizontal total, bits 9:8
1	Index 2, Horizontal display enable end, bits 9:8
2	Index 3, Horizontal blank start, bits 9:8
4	Index 5, Horizontal sync start, bits 9:8
6	Index 8, Vertical total, bits 11:8
12	Index 9, Vertical display enable end, bits 11:8
15	A, Vertical blank start, bits 11:8
10	Index C, Vertical sync start, bits 11:8
18	Index E, Line compare, bits 11:8
NOTE: The extended register bits are also reset on power-on reset.	

TABLE 15-44. WRITES TO VGA CRTC REGISTERS RESET EXTENDED REGISTER BITS

16.0 ATTRIBUTE CONTROLLER

16.1 OVERVIEW

The complete VGA Attribute Controller is supported, with both standard VGA and extended register access. The attribute controller receives slightly different handling through extended registers than other VGA blocks due to the manner in which the VGA Attribute Index register is implemented.

16.2 REGISTER MAP

The attribute controller registers are available through both VGA and extended register address spaces. The attribute controller registers are accessed through port 3C1h and 3C0h as follows:

PORT	FUNCTION
3C1h	Attribute Controller Data r/o
3C0h	Attribute Controller Index/Data

NOTE:
(1) Consecutive writes to port 3C0h toggle between Attribute Index and Attribute Data registers. Reading port 3?Ah resets the toggle to select the Attribute Index register.
(2) The Attribute Index register (port 3C0h) also contains an enable bit.

INDEX	FUNCTION
00	Palette Register 0
01	Palette Register 1
⇓	⇓
0F	Palette Register 15
10	Attribute Mode Control
11	Overscan Color
12	Color Plane Enable
13	Horizontal Pel Panning
14	Color Select

NOTE:
The Attribute Controller registers listed in this table are also accessible through the Register Access port using these same indices.

TABLE 16-1. ATTRIBUTE CONTROLLER REGISTERS, PORT 3C0/3C1

16.3 ATTRIBUTE INDEX REGISTER

BITS	FUNCTION
D7:6	Not Used
D5	Disable palette
D4:0	Index

NOTE:
This port is also a data port.

TABLE 16-2. ATTRIBUTE INDEX (VGA ACCESS ONLY), PORT 3C0h

D5	DISABLE PALETTE
1	Enable internal palette operation, disable writes to palette registers
0	Disable palette output, generate all 0's to RAMDAC, permit writes to palette registers

16.4 ATTRIBUTE CONTROLLER PALETTE REGISTERS

In 4-bit per pixel graphics mode and in text mode, the 4 bit pixel values read from display memory are translated through the attribute controller's palette. This palette is bypassed in 8-bit per pixel and higher modes, and can be bypassed in 4-bit mode through the VGA Disable Control register.

There are 16 attribute controller palette registers. Only the first and last registers are shown here.

BITS	FUNCTION
D7:6	Not Used
D5:0	Palette data 0

TABLE 16-3. PALETTE REGISTER 0, PORT 3C0h(WRITE) AND 3C1h(READ) INDEX 0

BITS	FUNCTION
D7:6	Not Used
D5:0	Palette data 15

TABLE 16-4. PALETTE REGISTER 15, PORT 3C0h(WRITE) AND 3C1h(READ) INDEX F

16.5 ATTRIBUTE MODE CONTROL REGISTERS

BITS	FUNCTION
D7	Override VID5:4
D6	PEL width 256
D5	PEL panning compatibility
D4	Not Used
D3	Enable Blink
D2	Enable line graphics character codes
D1	Enable MDA emulation
D0	Enable Graphics

TABLE 16-5. ATTRIBUTE MODE CONTROL, PORT 3C0h(WRITE) AND 3C1h(READ) INDEX 10

D7	OVERRIDE VID5:4
1	Color Select Register provides bits 5:4 to RAMDAC in 16-color modes
0	Palette provides bits 5:4 to RAMDAC in 16-color modes

D6	PEL WIDTH 256
1	Packed 256-color mode
0	Text or planar mode

D5	PEL PANNING COMPATIBILITY
1	Line compare match disables PEL panning for remainder of frame
0	Line compare has no effect on PEL panning

D3	ENABLE BLINK
1	Blink enabled by attribute bit 7
0	Blink disabled

D2	ENABLE LINE GRAPHICS CHARACTER CODES
1	In 9-dot character modes, 9th column of characters C0h through DFh are duplicated from 8th column
0	In 9-dot character modes, 9th column of all characters is blank
NOTE: This bit has no effect in 8-dot text or graphics modes.	

D1	ENABLE MDA EMULATION
1	Use MDA attributes
0	Use CGA/EGA attributes

D0	ENABLE GRAPHICS
1	Graphics (APA) mode
0	Text (alphanumeric) mode

16.6 ATTRIBUTE COLOR REGISTERS

The Overscan Color register specifies an 8-bit color to be displayed in the overscan (border) region when required.

BITS	FUNCTION
D7:0	Overscan color

TABLE 16-6. OVERSCAN COLOR, PORT 3C0h(WRITE) AND 3C1h(READ) INDEX 11

The Color Plane Enable register provides a mask into the 16-entry palette, and controls the video status multiplexer. A value of 0 in any bit position of the Color Plane Enable field forces the corresponding plane of 16-color VGA data to be set to 0 prior to indexing the palette. The Video Status Multiplexer field selects two of the eight bits at the output of the attribute controller to be made available for read at the Input Status register.

BITS	FUNCTION
D7:6	Not Used
D5:4	Video status multiplexer
D3:0	Color plane enable

TABLE 16-7. COLOR PLANE ENABLE, PORT 3C0h(WRITE) AND 3C1h(READ) INDEX 12

D5	D4	VIDEO STATUS MULTIPLEXER
1	1	Read VID7 & VID6 at Input Status register bits 5:4
1	0	Read VID3 & VID1 at Input Status register bits 5:4
0	1	Read VID5 & VID4 at Input Status register bits 5:4
0	0	Read VID2 & VID0 at Input Status register bits 5:4

The Color Select register specifies four color bits that can drive the RAMDAC inputs in certain modes. In 16-color planar modes, this register provides the 2 or 4 high-order bits of the color index send to the RAMDAC. In 256-color and higher modes, this register has no effect.

BITS	FUNCTION
D7:4	Not Used
D3:0	Color select (for VID 7:4)
NOTE: These bits can be written through the VGA Attribute Controller register block. Writing this register through VGA port 3C0h or 3C1h causes these bits to remain unchanged	

TABLE 16-8. COLOR SELECT, PORT 3C0h(WRITE) AND 3C1h(READ)) INDEX 14

16.7 HORIZONTAL PEL PANNING

BITS	FUNCTION
D7:4	Not Used
D3:0	Horizontal PEL panning

TABLE 16-9. HORIZONTAL PEL PANNING, 3C0h(WRITE) AND 3C1h(READ) INDEX 13

REGISTER VALUE	8-DOT	9-DOT	256-COLOR
8	--	0	--
7	7	8	--
6	6	7	3
5	5	6	--
4	4	5	2
3	3	4	--
2	2	3	1
1	1	2	--
0	0	1	0

TABLE 16-10. HORIZONTAL PEL PANNING VALUES

16.8 READING PORT 3C0h THROUGH EXTENDED REGISTERS

The attribute controller may be written and read through ports 3C0h and 3C1h in a VGA-compatible manner. When writing or reading these ports through the Register Access port, the following special criteria apply:

1. The toggling of 3C0h and 3C1h does not exist. Instead, the index is accessed on the high byte and the data on the low byte, in the same manner as conventional VGA index/data pairs.
2. Bit 5 of the Attribute Index register, which disables the internal palette, is loaded on every write to the Register Access port from bit 5 in the high byte of the port.
3. When chain reading this register block, bit 5 of the Attribute Index register is returned on every read from the Register Access port in bit 5 in the high byte of the port. Regardless of the value of this bit, a read past index 14h of this register block returns the transition code (index F0) of the next register block.

BITS	FUNCTION
D15	Must be 0
D14	Not Used
D13	Attribute controller index register bit 5
D12:8	Index of specific register (00-14h)
D7:0	Data for specific register
NOTE: Some registers have less than 8 bits.	

TABLE 16-11. ATTRIBUTE CONTROLLER REGISTERS (EXTENDED REGISTER ACCESS), BLOCK 30

16.9 LOCKING THE VGA ATTRIBUTE CONTROLLER REGISTERS

When the Lock VGA Attribute Controller Registers bit is set in the VGA Lock Control register, the following VGA attribute controller registers are locked from writes via the VGA registers (port 3C0/1). All registers are always writable through the VGA Attribute Controller register block.

INDEX	FUNCTION
00	Palette Register 0, bits 5:0
⇓	⇓
0F	Palette Register 15, bits 5:0
10	Attribute Mode Control, bit 7
11	Overscan Control, bits 7:0
12	Color Plane Enable, bits 3:0

TABLE 16-12. LOCKABLE ATTRIBUTE CONTROLLER REGISTERS BITS

17.0 GRAPHICS CONTROLLER

17.1 OVERVIEW

The complete VGA Graphics Controller is supported, with both standard VGA and extended register access.

17.2 REGISTER MAP

The graphics controller registers are available through both VGA and extended register address spaces. The graphics controller register access ports are as follows:

PORT	FUNCTION
3CFh	Graphics Controller Data
3CEh	Graphics Controller Index

INDEX	FUNCTION
0	Set/reset
1	Enable Set/Reset
2	Color Compare
3	Data Rotate
4	Read Map Select
5	Graphics Mode
6	Miscellaneous
7	Color Don't Care
8	Bit Mask

NOTE:
The VGA Graphics Controller registers are also accessible through the Register Access port using these same indices.

TABLE 17-1 VGA GRAPHICS CONTROLLER REGISTERS, PORT 3CEh/3CFh

17.3 GRAPHICS INDEX REGISTER

BITS	FUNCTION
D7:4	Not Used
D3:0	Index

TABLE 17-2. GRAPHICS INDEX (VGA ACCESS), PORT 3CEh

17.4 SET/RESET AND ENABLE REGISTERS

The Set/Reset and Enable Set/Reset register are used in VGA writes modes 0 and 3 to specify 4-bit colors to be written in planar modes.

BITS	FUNCTION
D7:4	Not Used
D3:0	Set/reset map 3:0

TABLE 17-3. SET/RESET, PORT 3CFh INDEX 0

BITS	FUNCTION
D7:4	Not Used
D3:0	Enable set/reset map 3:0

TABLE 17-4. ENABLE SET/RESET, PORT 3CFh INDEX 1

17.5 COLOR COMPARATOR REGISTERS

The Color Compare and Color Don't Care registers specify a 4-bit color and mask to be used when the Read Type bit of the Graphics Mode register selects reading display memory through the color comparators.

BITS	FUNCTION
D7:4	Not Used
D3:0	Color compare map 3:0

TABLE 17-5. COLOR COMPARE, PORT 3CFh INDEX 2

BITS	FUNCTION
D7:4	Not Used
D3:0	Color don't care map 3:0

TABLE 17-6. COLOR DON'T CARE, PORT 3CFh INDEX 7

17.6 DATA ROTATE AND BIT MASK REGISTERS

The Data Rotate register specifies rotation for write modes 0 and 3 and raster operations for write modes 0, 2, and 3

BITS	FUNCTION
D7.5	Not Used
D4 3	Function select
D2 0	Rotate count (0-7)

TABLE 17-7. DATA ROTATE, PORT 3CFh INDEX 3

D4	D3	FUNCTION SELECT
1	1	Source XOR read-back latches
1	0	Source OR read-back latches
0	1	Source AND read-back latches
0	0	Source copy

The Bit Mask register specifies which 4-bit pixels should be written form the read-back latch and which from the CPU data in write modes 0, 2, and 3

BITS	FUNCTION
D7 0	Bit mask planes 7:0

TABLE 17-8. BIT MASK, PORT 3CFh INDEX 8

17.7 GRAPHICS MODE, READ MAP, AND MISCELLANEOUS REGISTERS

The Read Map Select register specifies which of the four maps should be read in planar modes when the Read-Type bit of the Graphics Mode register is reset.

BITS	FUNCTION
D7:2	Not Used
D1:0	Map select (0-3)

TABLE 17-9. READ MAP SELECT, PORT 3CFh INDEX 4

BITS	FUNCTION
D7	Not Used
D6:5	Graphics mode
D4	Odd/even
D3	Read type
D2	Not Used
D1:0	Write mode

TABLE 17-10. GRAPHICS MODE, PORT 3CFh INDEX 5

D6	D5	GRAPHICS MODE
1	1	Not Used
1	0	Packed mode (VGA mode 13)
0	1	CGA-compatible modes (VGA mods 4 & 5)
0	0	Basic text and graphics modes

D4	ODD/EVEN
1	Chain 2 addressing (VGA modes 0-5)
0	Unchained or chain 4 addressing

D3	READ TYPE
1	Read from color comparators
0	Read directly from memory

D1	D0	WRITE MODE
1	1	Write data from Set/Reset register. Rotated CPU data 7:0 AND'ed with Bit Mask register masks the data.
1	0	Write data from CPU data 3:0. Bit Mask register masks the data.
0	1	Write data from 32-bit read-back latch.
0	0	For any map with Enable Set/ Reset register bit set, write value in corresponding Set/Reset register bit. Where Enable Set/ Reset is not set, write corresponding rotated CPU data. Bit Mask register masks the data.

BITS	FUNCTION
D7:4	Not Used
D3:2	CPU aperture(1)
D1	Odd/even
D0	Graphics mode
NOTE: The CPU aperture bits (D3:2) can be overridden in the Aperture Control register	

TABLE 17-11. MISCELLANEOUS, PORT 3CFh INDEX 6

D3	D2	CPU APERTURE
1	1	CPU address is B800:0 to BFFF:F (32k bytes)
1	0	CPU address is B000:0 to B7FF:F (32k bytes)
0	1	CPU address is A000:0 to AFFF:F (64k bytes)
0	0	CPU address is A000:0 to BFFF:F (128k bytes)

D1	ODD/EVEN *** OTHER BITS USED ***
1	Chain 2 addressing
0	Unchained or chain 4 addressing

D0	GRAPHICS MODE
1	Graphics mode
0	Alphanumeric mode

17.8 LOCKING THE VGA GRAPHICS CONTROLLER REGISTERS

When the Lock VGA Graphics Controller Registers bit is set in the VGA Lock Control register, all VGA graphics controller registers are locked from writes via the VGA registers (port 3CE/F). All registers are always writable through the VGA Graphics Controller register block.

17.9 ACCESSING THE VGA GRAPHICS CONTROLLER REGISTERS THROUGH EXTENDED REGISTERS

The graphics controller may be written and read through ports 3CE and 3CF in a VGA-compatible manner. They may also be accessed through the extended registers as follows:

BITS	FUNCTION
D15:12	Must be 0
D11:8	Index of specific register (0-8h)
D7:0	Data for specific register
NOTE: Some registers have less than 8 bits.	

TABLE 17-12. GRAPHICS CONTROLLER REGISTERS (EXTENDED REGISTER ACCESS), BLOCK 32

18.0 SEQUENCER

18.1 OVERVIEW

The complete VGA Sequencer is supported, with both standard VGA and extended register access.

18.2 REGISTER MAP

The sequencer registers are available through both VGA and extended register address spaces. The sequencer register ports are as follows:

PORT	FUNCTION
3C5h	Sequencer Data
3C4h	Sequencer Index

INDEX	FUNCTION
0	Reset *** not supported ***
1	Clocking mode
2	Map mask
3	Character map select
4	Memory mode
NOTE: The VGA Sequencer registers are also accessible through the Register Access port using these same indices.	

TABLE 18-1. VGA SEQUENCER REGISTERS, PORTS 3C4h AND 3C5h

18.3 SEQUENCER INDEX REGISTER

BITS	FUNCTION
D7:4	Not Used
D3:0	Index

TABLE 18-2. SEQUENCER INDEX (VGA ACCESS), PORT 3C4h

18.4 SEQUENCER DATA REGISTER

BITS	FUNCTION
D7:2	Not Used
D1	Asynchronous reset
D0	Synchronous reset

TABLE 18-3. RESET, PORT 3C5h INDEX 0

D1	D0	RESET ***VGA FUNCTION NOT SUPPORTED ***
1	1	Sequencer operational
X	0	Sequencer halted (asynchronous)
0	X	Sequencer halted (synchronous)

BITS	FUNCTION
D7:6	Not Used
D5	Screen off
D4,2	Shift load
D3	Dot clock
D1	Not Used
D0	8/9 dot clock select

TABLE 18-4. CLOCKING MODE, PORT 3C5h INDEX 1

D5	SCREEN OFF
1	Screen off, but sync remains active
0	Screen on

D4	D2	SHIFT LOAD *** VGA FUNCTION NOT SUPPORTED ***
1	X	Video serializer loaded once per four character clocks
0	1	Video serializer loaded once per two character clocks
0	0	Video serializer loaded once per character clock

D3	DOT CLOCK
1	Pixel clock is input VCLK divided by 2
0	Pixel clock is input VCLK

D0	8/9 DOT CLOCK SELECT
1	Character clock is input VCLK divided by 8
0	Character clock is input VCLK divided by 9

BITS	FUNCTION
D7:4	Not Used
D3:0	Map mask, planes 3:0

TABLE 18-5. MAP MASK, PORT 3C5h INDEX 2

D3/D0	MAP MASK, PLANES 3/0
1	Writing to map enabled
0	Writing to map disabled

BITS	FUNCTION
D7:6	Not Used
D5, D3, D2	Character map select A
D4, D1, D0	Character map select B

TABLE 18-6. CHARACTER MAP SELECT, PORT 3C5h INDEX 3

D3	D2	D5	CHARACTER MAP SELECT A
1	1	1	8th 8k byte block
1	1	0	7th 8k byte block
⇓			⇓
0	0	1	2nd 8k byte block
0	0	0	1st 8k byte block

D1	D0	D4	CHARACTER MAP SELECT B
1	1	1	8th 8k byte block
1	1	0	7th 8k byte block
⇓			⇓
0	0	1	2nd 8k byte block
0	0	0	1st 8k byte block

BITS	FUNCTION
D7:6	Not Used
D3	Chain 4 mode
D2	Odd/even addressing mode
D1	Extended memory
D0	Not Used

TABLE 18-7. MEMORY MODE, PORT 3C5h INDEX 4

D3	CHAIN 4 MODE
1	Chain 4 addressing mode enable
0	Sequential addressing mode enable

D2	ODD/EVEN ADDRESSING MODE
1	Sequential addressing mode enabled
0	Odd/even addressing mode enable

D1	EXTENDED MEMORY
1	Greater than 64k bytes of video memory available
0	64k bytes of video memory available

18.5 LOCKING THE VGA SEQUENCER REGISTERS

When the Lock VGA Sequencer Registers bit is set in the VGA Lock Control register, all VGA sequencer registers are locked from writes via the VGA registers (port 3C4/5). All registers are always writable through the VGA Sequencer register block.

18.6 ACCESSING THE VGA SEQUENCER REGISTERS THROUGH EXTENDED REGISTERS

The sequencer may be written and read through ports 3C4 and 3C5 in a VGA-compatible manner. They may also be accessed through the extended registers as follows:

BITS	FUNCTION
D15:11	Must be 0
D10:8	Index of specific register (0-4h)
D7:0	Data for specific register(1)
NOTE: Actual registers have less than 8 bits.	

TABLE 18-8. SEQUENCER REGISTERS (EXTENDED REGISTER ACCESS), BLOCK 31

19.0 GENERAL REGISTERS

19.1 REGISTER MAP

PORT (HEX)	FUNCTION
	MONITOR
3C2	Miscellaneous Output register(5)
3CC	Miscellaneous Output register(6)
3?A(1)	Feature Control register(5)
3CA	Feature Control register(6)
3C2	Input Status Register 0(6)
3?A	Input Status Register 1(2)(6)
	RAMDAC REGISTERS
3C6	RAMDAC Pixel Mask
3C7	RAMDAC Read Address(5)
3C7	RAMDAC State
3C8	RAMDAC Write Address
3C9	RAMDAC Data
	SETUP REGISTERS
46E8(3)	AT Mode Setup
102(3)	Wake-up VGA
	PCI CONFIGURATION REGISTERS
0(4)	PCI Configuration ID
4(4)	PCI Configuration Status/ Command
8(4)	PCI Configuration Class Code
10(4)	PCI Linear Address Map Starting Address
30(4)	PCI Expansion ROM Base Address
3C(4)	PCI Interrupt Control

TABLE 19-1. GENERAL VGA AND SETUP REGISTERS

PORT (HEX)	FUNCTION

NOTE:

(1) Port 3CCh bit 0 selects 3BAh or 3DAh for this port.

(2) Reading this port also resets port 3C0h for index writes.

(3) These port addresses are a guide only. See the section on VGA Setup Registers for complete information.

(4) These register can only be accessed in the PCI configuration space.

(5) These registers are write/only.

(6) These registers are read/only

TABLE 19-1. GENERAL VGA AND SETUP REGISTERS (Continued)

19.2 MISCELLANEOUS OUTPUT AND FEATURE CONTROL REGISTERS

BITS	FUNCTION
D7	Vertical sync polarity select
D6	Horizontal sync polarity select
D5	Odd/even memory page select
D4	(reserved)
D3:2	Video clock select(1)(2)
D1	Enable video RAM
D0	I/O address select

NOTES:

(1) Writing to port 3C2h may modify certain bits in the Clock Generator Interface register and may automatically generate a register load cycle to the clock generator.

(2) Bits D3:2 cannot be written if the Lock Port 3C2h bit is set in the Clock Generator Interface register.

TABLE 19-2. MISCELLANEOUS OUTPUT, PORT 3C2h (WRITE) AND 3CCh(READ)

D7	VERTICAL SYNC POLARITY SELECT
1	Sync polarity is negative
0	Sync polarity is positive

D6	HORIZONTAL SYNC POLARITY SELECT
1	Sync polarity is negative
0	Sync polarity is positive

D5	ODD/EVEN MEMORY PAGE SELECT
1	Upper 64k byte page selected
0	Lower 64k byte page selected

D3	D2	VIDEO CLOCK SELECT
1	1	(reserved)
1	0	Select programmable VCLK (VSEL frequency select 10b)*
0	1	Select VCLK1 (VSEL frequency select 01b)*
0	0	Select VCLK0 (VSEL frequency select 00b)*
*Refer to Table 13-3.		

D1	ENABLE VIDEO RAM
1	CPU access to video memory enabled
0	CPU access to video memory disabled

D0	I/O ADDRESS SELECT
1	Color addresses selected (3DXh)
0	Monochrome addresses selected (3BXh)

BITS	FUNCTION
D7:4	(reserved)
D3	Vertical sync control
D2:0	(reserved)

TABLE 19-3. FEATURE CONTROL, PORT 3?Ah (WRITE) AND 3CAh(READ)

D3	VERTICAL SYNC CONTROL
1	VSYNC is logical OR if VSYNC and Vertical Display Enable
0	VSYNC output enabled

19.3 INPUT STATUS REGISTERS

BITS	FUNCTION
D7	CRT interrupt
D6:5	(reserved)
D4	Monitor detect (MDET)*
D3:0	(reserved)

NOTE:
*For bit D4, MDET is the default use. However, if Block 38 Index 8, bit D2 is set to 1, bit D4 is used for USR4.

TABLE 19-4. INPUT STATUS REGISTER 0, READ/ONLY PORT 3C2h

D7	CRT INTERRUPT
1	Vertical retrace interrupt pending
0	Vertical retrace interrupt cleared

D4	MONITOR DETECT
1	Color monitor detected
0	Monochrome monitor detected

NOTE:
When external RAMDAC is used, this bit returns the MDET. When internal RAMDAC is used, bit returns value from internal comparators

BITS	FUNCTION
D7:6	(reserved)
D5:4	Diagnostic
D3	Vertical retrace
D2:1	(reserved)
D0	Display enabled

TABLE 19-5. INPUT STATUS REGISTER 1, READ/ONLY PORT 3?Ah

D5:4	DIAGNOSTIC
Returns two of eight video outputs selected by Color Plane Enable register bits 5:4	

D3	VERTICAL RETRACE
1	Vertical retrace is active
0	Vertical frame is displayed

D0	DISPLAY ENABLED
1	CRT screen display disabled for horizontal or vertical retrace
0	CRT screen display in progress

19.4 RAMDAC REGISTERS

The RAMDAC interface is mapped into the following registers:

PORT (HEX)	FUNCTION
3C9	RAMDAC Data
3C8	RAMDAC Write Address
3C7	RAMDAC State (when read)
3C7	RAMDAC Read Address (when written)
3C6	RAMDAC Pixel Mask
NOTE: Port 3C7h is maintained by the controller and does not cause a RAMDAC access when read.	

TABLE 19-6. VGA RAMDAC REGISTERS

PORT 3C7h	RAMDAC STATE
03	Port 3C7h was written more recently than port 3C8h
00	Port 3C8h was written more recently than port 3C7h

When the RAMDAC Shadowing Control field of the RAMDAC Interface register specifies RAMDAC shadowing, all RAMDAC writes from the host take place, but the $\overline{LDEV}$ signal is not asserted, causing any secondary RAMDAC on the AT/MCA bus to also receive the write operation.

When shadowing is in effect, RAMDAC reads from the host are either performed, in which case $\overline{LDEV}$ is asserted; or ignored, in which case $\overline{LDEV}$ is not asserted, depending on the setting of the RAMDAC Shadowing Control field.

19.5 VGA SETUP REGISTERS

BITS	FUNCTION
D7:6	Not Used
D4	Setup
D3	Enable I/O and memory accesses
D2:0	Not Used
NOTE: (1) The same bits are decodes at ports 46E8h, 56E8h, 66E8h, and 76E8h. (2) In standard VGA, bits D2:0 were the External BIOS ROM Page Select	

TABLE 19-7. HOST BUS MODE SETUP, PORT46E8h

D4	D3	SETUP AND ENABLE I/O AND MEMORY ACCESS
0	0	Only register 46E8h is accessible
0	1	All registers and memory except port 102h accessible
1	X	Only port 102h accessible

BITS	FUNCTION
D0	Wake-up VGA
D7:1	Not Used
NOTE: In AT mode, this register can be written only when the Setup bit in the AT Mode Setup register is set. In MCA mode, this register can be written when the CDSETUP- line is asserted. This port decodes to all address locations ending in 010 (binary)	

TABLE 19-8. WAKEUP VGAPORT 102h

D0	WAKEUP VGA
1	VGA awake
0	VGA asleep

19.6 PCI SETUP REGISTERS

The following PCI setup registers are accessible only in the configuration space of PCI.

BITS	FUNCTION
D31:16	9710 (device ID)
D15:0	101Ch (vendor ID)
NOTE: Bits D31:0 are read/only bits.	

TABLE 19-9. PCI CONFIGURATION ID, PCI CONFIGURATION PORT 0

BITS	FUNCTION
D31:28	0000
D27	0 (target abort status)
D26:25	Response Timing
	01 if Configuration Bit 20 = 0
	10 if Configuration Bit 20 = 1
D24:16	0 0000 0000
D15:6	Not Used
D5	Palette snoop enable
D4:2	Not Used
D1	Memory enable
D0	I/O enable
NOTE: Bits D31:16 are read/only bits.	

TABLE 19-10. PCI CONFIGURATION STATUS/ COMMAND, PCI CONF PORT 4

BITS	FUNCTION
D31:8	03 00 00 (class code)
D7:0	Revision code
NOTE: (1) Bits D31:0 are read/only bits. (2) Bits D7:0 match the revision code in CRTC register 39.	

TABLE 19-11. PCI CONFIGURATION CLASS CODE, PCI CONF PORT 8

BITS	FUNCTION
D31:22	Base Address
D21:4	Not Used
D3:0	Type 0 Memory Space
NOTE: Bits D31:22 can be read and written, but bits D3:0 are read/only.	

TABLE 19-12. PCI CONFIGURATION LINEAR ADDRESS BASE ADDRESS, PCI CONFIGURATION PORT 10

BITS	FUNCTION
D31:15	Expansion ROM base address (upper bits)
D14:1	Not Used
D0	Address decode enable

TABLE 19-13. PCI CONFIGURATION EXPANSION ROM BASE ADDRESS, PCI CONFIGURATION PORT 30

BITS	FUNCTION
D31:16	Not Used
D15:8	0000 0001 (interrupt pin) *r/o*
D7:0	Interrupt line
NOTE: Bits D15:8 are read/only.	

TABLE 19-14. PCI CONFIGURATION INTERRUPT CONTROL, PCI CONFIGURATION PORT 3C

All other PCI configuration registers return all zeroes when read.

20.0 SIGNATURE ANALYZER

20.1 OVERVIEW

The Signature Analyzer generates a 16-bit polynomial signature of the video data being input to or output from the internal palette RAM. The signature includes all visible pixels, as well as the current timing information. The actual sync and blank outputs may optionally be included. In interlaced mode, the signature always encompasses an entire frame.

20.2 REGISTER MAP

INDEX	FUNCTION
0	Analyzer Control
1	Analyzer Signature Low
2	Analyzer Signature High
NOTE: Indexes 1 and 2 are read/only registers.	

TABLE 20-1. SIGNATURE ANALYZER REGISTERS, BLOCK 14

20.3 CONTROL AND STATUS

BITS	FUNCTION
D15:12	0000 (index)
D11	Analyzer enable/status *rst*
D10	Analyzer interrupt enable *rst*
D9	Analyzer reset
D8:7	Analyzer input select
D6:4	Analyzer video source select
D3:2	Not Used
D1	RGB Feedback Select
D0	RGB Feedback Control
NOTE: Bits D11 and D10 are reset at power-on and reset.	

TABLE 20-2. ANALYZER CONTROL, BLOCK 14 INDEX 0

D11	ANALYZER ENABLE/STATUS
1	Start analyzer/analysis in progress
0	Stop analyzer/analysis complete

D10	ANALYZER INTERRUPT ENABLE
1	Interrupt on completion of analysis
0	Analyzer interrupt disabled

D9	ANALYZER RESET
1	Reset analyzer to seed value when analysis begins
0	Do not reset analyzer to seed value when analysis begins

D8	D7	ANALYZER INPUT SELECT
1	1	Source is screen pixels combined with screen timing signals
1	0	Source is screen timing signals only
0	1	Source is screen pixels from video source only
0	0	Source is null

D6	D5	D4	ANALYZER VIDEO SOURCE SELECT
X	1	1	Video source is null (all zeroes)
1	1	0	Video source is red input to RAM
1	0	1	Video source is green input to RAM
1	0	0	Video source is blue input to RAM
0	1	0	Video source is blue output from RAM
0	0	1	Video source is green output from RAM
0	0	0	Video source is red output from RAM

D1	RGB FEEDBACK SELECT
1	Odd Pixel Selected
0	Even Pixel Selected

NOTE:
In double pixel mode, two pixels are output simultaneously, but the Signature Analyzer can only sample one pixel. This bit selects the bit that is sampled. In single pixel mode, this bit is not used.

D0	RGB FEEDBACK CONTROL
1	Feedback Value is 0
0	Feedback Value (Preset) is Enabled

20.4 SIGNATURE VALUES

BITS	FUNCTION
D15:12	0001 (index)
D11:8	Not Used
D7:0	Low byte of analyzer signature

TABLE 20-3. ANALYZER SIGNATURE LOW, R/O BLOCK 14 INDEX 1

BITS	FUNCTION
D15:12	0010 (index)
D11:8	Not Used
D7:0	High byte of analyzer signature

TABLE 20-4. ANALYZER SIGNATURE HIGH, R/O BLOCK 14 INDEX 2

20.5 ANALYZER VIDEO SOURCE SELECTION

The Analyzer Video Source Select and Input Select fields of the Analyzer Control register together specify what input data is passed through the analyzer and thus affect the signature.

All pixel clock times in a video frame (defined by VSYNC) are included in the signature. The input source selection affects the data to the analyzer as follows:

BIT	SOURCE
VIDEO INPUT IS NULL	
D7:0	0000 0000
	VIDEO INPUT IS SCREEN PIXELS ONLY...
D7:0	Video source(1) bits 7:0
VIDEO INPUT IS SCREEN TIMING ONLY	
D7:4	0000
D3	Odd frame(2)
D2	BLANK-
D1	HSYNC-
D0	VSYNC-
VIDEO INPUT IS SCREEN PIXELS AND SCREEN TIMING	
D7:4	Video source(1) bits 7:4
D3	Video source(1) bit 3 XOR Odd frame(2)
D2	Video source(1) bit 2 XOR BLANK-
D1	Video source(1) bit 1 XOR HSYNC-
D0	Video source(1) bit 0 XOR VSYNC-

NOTE:
(1) This is the byte selected by the Analyzer Video Source Select field
(2) This bit is 1 during odd fields in interlaced mode, 0 during even fields and in non-interlaced mode

TABLE 20-5. ANALYZER INPUTS

20.6 GENERATING A SIGNATURE

Analysis begins when the Analyzer Enable bit is set in the Analyzer Control register. This bit is reset by the WD9710 to signal analysis complete. Analysis may be interrupted by writing the register with this bit reset, in which case the signature registers contains invalid data.

If the Analyzer Interrupt Enable bit is set in the Analyzer Control register, an interrupt is generated when the analysis is complete.

When the analysis complete, the host may read the 16-bit signature from the Analyzer Signature Low and High registers.

After the Analyzer Enable bit is set, actual analysis is synchronized to the next complete frame, so completion times vary depending on when the bit was set.

20.7 ANALYZING IN INTERLACED MODE

In interlaced mode, all signature calculations begin at the start of an odd field, and finish at the end of an even field. Interrupts, if any, are generated only at the end of the even field.

NOTE

The signature of any picture differs if analyzed in interlaced or non-interlaced mode. Also, the signature of a picture analyzed in interlaced mode varies depending on the vertical placement of the picture. The cursor, if displayed, is included in the signature; as is any blinking on the screen.

20.8 DESCRIPTION OF SIGNATURE

The signature for each frame is calculated as follows:

When the Analyzer Reset bit is set in the Analyzer Control register, the internal signature is set to a seed value of 0001h at the start of signature collection. When this bit is reset, the existing value in the signature registers is used as a seed value.

The polynomial generated by the analyzer is-

$$(x^{16} + x^{12} + x^5 + 1),$$

which is the CRC-CCITT polynomial.

21.0 SCRATCHPAD REGISTERS

21.1 OVERVIEW

The WD9710 has a dedicated group of 8-bit scratchpad registers available for use by the BIOS. These registers perform no internal function other than being writable and readable.

While a theoretical maximum of 240 8-bit scratchpad registers could be defined, the actual number implemented on a given WD9710 is usually lower. The actual number of physical scratchpad registers available can be read upon reset in scratchpad register 00.

21.2 REGISTER MAP

INDEX	FUNCTION
00	Scratchpad register 0(1)
01	Scratchpad register 1 (2)
02	Scratchpad register 2
⇓	⇓
nn	Scratchpad register 'nn'(3)

NOTES:

(1) On reset, this register contains the index of the highest-numbered scratchpad register available

(2) On reset, this register is loaded from configuration bits CNF63:56

(3) The number of available scratchpad registers may vary

TABLE 21-1. SCRATCHPAD REGISTERS, BLOCK 16

21.3 USE OF SCRATCHPAD REGISTERS

Scratchpad registers are read and written like 8-bit VGA registers, as follows:

BITS	FUNCTION
D15:8	'nn' (index)
D7:0	Scratchpad

TABLE 21-2. SCRATCHPAD REGISTER 'nn', BLOCK 16 INDEX 'nn'

22.0 PARADISE REGISTERS SUPPORTED

22.1 REGISTER MAP

PORT (HEX)	INDEX (HEX)	REGISTER NAME
3CF	09	PR0A Address Offset A
3CF	0A	PR0B Address Offset B
3CF	0B	PR1 Memory Size-bit 3
3C5	11	PR31 System Interface Control-bit 7
3D5	31-39	WD Chip ID registers *r/o*
NOTE: Offset registers A and B share space with the 12-bit Extended Address Offset registers in the General Registers register block		

TABLE 22-1. PARADISE REGISTERS SUPPORTED

22.2 ADDRESS OFFSET REGISTERS

The Address Offset A and B registers specify offsets in 4k byte chunks to be added to the CPU address during read and write operations. These registers permit access of display memory regions larger than the current aperture.

The Extended Address Offset A and B registers in the System Control Registers register block share space with these two registers. Writing either of the extended registers overwrites the 8 bits of PR0A or PR0B. Writing either PR0A or PR0B automatically resets the four high-order bits of both of the Extended Address Offset registers. There is no register locking between these registers.

BITS	FUNCTION
D7:0	Primary address offset, in 4k byte chunks

TABLE 22-2. PR0A ADDRESS OFFSET A, PORT 3CFh INDEX 09h

BITS	FUNCTION
D7:0	Secondary address offset, in 4k byte chunks

TABLE 22-3. PR0B ADDRESS OFFSET B, PORT 3CFh INDEX 0Ah

When the Enable PR0B bit in the PR1 Memory Size register is reset, PR0A is used as the offset for all CPU access. Otherwise, PROA or PR0B may be used, as follows:

When the Read/Write Offset bit is reset in the PR31 System Interface Control register, and when the display memory aperture is set to 128k byte, then PR0B is the used as the offset for the lower 64k byte, and PR0A is used for the upper 64k byte. When the Enable PR0B bit is set, and when the display memory aperture is set to 64k byte or 32k byte, then PR0B is the used as the offset for the lower 32k byte, and PR0A is used for the upper 32k byte, if any.

When the Read/Write Offset bit is set then PR0B is used as the offset for CPU write operations and PR0A is used for CPU reads.

BITS	FUNCTION
D7:4	(used in previous Paradise chips but not used here)
D3	Enable PR0B
D2:0	(used in previous Paradise chips but not used here)

TABLE 22-4. PR1 MEMORY SIZE, PORT 3CF INDEX 0B

D3	ENABLE PR0B
1	Use PR0A and PR0B as the offset registers
0	Use only PR0A as the offset register

BITS	FUNCTION
D7	Read/write offset enable
D6:0	(used in previous Paradise chips but unused here)

TABLE 22-5. PR31 SYSTEM INTERFACE CONTROL, PORT 3C5 INDEX 11

22.3 CHIP ID REGISTER

The WD9710 supports nine read-only chip ID registers. Table 22-7 lists a typical chip ID register.

BITS	FUNCTION
D7:0	57h (ASCII code for "W") *r/o*

TABLE 22-6. CHIP ID REGISTER 1, PORT 3D5 INDEX 31

The complete set of chip ID registers contains the ASCII values to output the string "WD9710 xx" where "xx" is the revision code of the chip, starting at 00.

23.0 NON-VGA REGISTER COMPATIBILITY

23.1 PRE-VGA REGISTERS

The following MDA, CGA, EGA, 6845, AT&T, and Hercules registers are not supported on the WD9710. Writing these registers has no effect and reading them returns unknown data.

PORT (HEX)	REGISTER	SUPPORT
3B8/ 3D8	Mode Control (all), write/only	None
3D9	Color select register (CGA, AT&T), write/only	None
3BA/ 3DA	Status (all), read/only	Keep VGA Portions
3B9	Preset light pen latch (MDA), write/only	None
3DB	Preset light pen latch (CGA, AT&T), write/only	None
3BB/ 3DB	Clear light pen latch (MDA, CGA, AT&T), write/ only	None
3DE	AT&T/M24 register (AT&T), write/only	None
3BF	Hercules register (Hercules), (write/only	None
3B0- 3B7	6845 registers (MDA, Hercules)	None
3D0- 3D7	6845 registers (CGA, AT&T)	None

TABLE 23-1. PRE-VGA REGISTERS

23.2 PARADISE REGISTERS

The Paradise registers listed in Table 23-2 are included in many previous chip designs. However, these Paradise registers have minimal or no support in the WD9710 chip design. Some of these register functions are supported in different ways, usually by consolidating similar bits into new extended registers.

REGISTER NO.	REGISTER NAME	PORT (HEX)	INDEX (HEX)	SUPPORT
PR0A	Address offset A	3CF	09	Yes
PR0B	Address offset B	3CF	0A	Yes
PR1	Memory size	3CF	0B	Bit 3 Only
PR2	Video select	3CF	0C	None
PR3	CRT control	3CF	0D	None
PR4	Video control	3CF	0E	None
PR5	Unlock PR0-4/Status	3CF	0F	None(1)
PR10	Unlock PR11-17	3?5	29	None
PR11	EGA switches	3?5	2A	None(1)
PR12	Scratch pad	3?5	2B	None(2)
PR13	Interlace H/2start	3?5	2C	move
PR14	Interlace H/2 end	3?5	2D	None
PR15	Miscellaneous control 1	3?5	E	None
PR16	Miscellaneous control 2	3?5	2F	None
PR17	Miscellaneous control 3	3?5	30	None
---	Register ID 1	3?5	31	Yes
⇓	⇓	⇓	⇓	⇓
---	Register ID 12	3?5	3C	Yes
PR1A	CRTC shadow register control	3?5	3D	None
PR18	CRTC vertical timing overflow	3?5	3E	None
PR19	Signature analyzer control	3?5	3F	move
PR20	Unlock sequencer extended registers	3C5	06	None
PR21	Display configuration/scratch pad	3C5	07	None(2)
PR22	Scratch pad	3C5	08	None(2)
PR23	Scratch pad	3C5	09	None(2)
PR30	Memory interface/write buffer/FIFO control	3C5	10	None
PR31	System interface control	3C5	11	Bit 7 Only
PR32	Miscellaneous control 4	3C5	12	None
PR33	DRAM timing/0WS control	3C5	13	None
PR34	Video memory mapping	3C5	14	None
PR35	(reserved)	3C5	15	None

NOTE:
(1) Register is not supported but configuration bits are readable elsewhere.
(2) A consecutive block of scratchpad registers exists elsewhere.

TABLE 23-2. PARADISE REGISTERS

23.3 SHADOW REGISTERS

The CRTC shadow registers present in some previous chips are not supported.

PORT (HEX)	INDEX (HEX)	DESCRIPTION	SUPPORT
3?5	00	Horizontal total	None
3?5	02	Horizontal Blank Start	None
3?5	03	Horizontal Blank End	None
3?5	04	Horizontal Sync Start	None
3?5	06	Vert total	None
3?5	07	Overflow Vertical	None
3?5	09	Maximum scan line	None
3?5	10	Vert sync start	None
3?5	11	Vert sync end	None
3?5	15	Vert blank start	None
3?5	16	Vert blank end	None

TABLE 23-3. SHADOW REGISTERS

23.4 TEST REGISTERS

The test registers present in previous chips are not supported, however new test registers are present.

PORT	INDEX	DESCRIPTION	SUPPORT
3?5	20	Test register 0	None
3?5	21	Test register 1	None
3?5	22	Test register 2	None
3?5	23	Test register 3	None
3?5	24	Test register 4	None
3?5	25	Test register 5	None
3?5	26	Test register 6	None
3?5	27	Test register 7	None
3?5	28	Test register 8	None

TABLE 23-4. TEST REGISTERS

24.0 SYSTEM CONTROL REGISTERS

24.1 REGISTER MAP

INDEX	FUNCTION
00	Master reset
01	Host interface
02	Power-down control
03	Display memory configuration - part 1
04	Display memory configuration - part 2
05	Display memory configuration - part 3
06	RAMDAC interface
07	VAFC connector interface
08	Monitor interface
09	Interlace control
0A	I/O re-mapping
0B	VGA lock control
0C	VGA override control
0D	VGA disable control
0E	Tri-state control - part 1
0F	Tri-state control - part 2
10	Display memory aperture
11	Display memory linear start address
12	ROM interface register
13	Video FIFO control
14	Companion Chip Interface
15	USR Pins Register

TABLE 24-1. SYSTEM CONTROL FUNCTIONS - CONFIGURATION, BLOCK 0

INDEX	FUNCTION
00	Interrupt status
NOTE: This is a read/only register.	

TABLE 24-2. SYSTEM CONTROL FUNCTIONS - STATUS, R/O BLOCK 1

INDEX	FUNCTION
0	Extended address offset A
1	Extended address offset B

TABLE 24-3. SYSTEM CONTROL FUNCTIONS - EXTENSION, BLOCK 2

24.2 CHIP RESET

BITS	FUNCTION
D15:8	0000 0000 (index)
D7:1	Not Used
D0	Master reset
NOTE: (1) Writing a 1 to bit D0 resets the internal sequencer and many on-chip registers. Bit D0 then automatically resets to 0. (2) Bit D0 is reset at power-on and reset.	

TABLE 24-4. MASTER RESET, BLOCK 0 INDEX 00

24.3 HOST INTERFACE

The WD9710 can be interfaced to the host through the AT bus, 486/VL-bus, or PCI bus. These bits are set at power-on, and while writable for test purposes, should not be written.

BITS	FUNCTION
D15:8	0000 0001 (index)
D7	Enable vertical retrace interrupt
D6	AT bus 16-bit interface
D5	Zero wait state disable
D4	Burst mode enabled
D3	Video port / VAFC connector
D2	Multiplexed host address/data bus
D1:0	Host interface

NOTES:
(1) Bits D7 and D6 are reset at power-on and reset.
(2) Bits D2:0 are read-only.
(3) Bits D5:0 are set at power-on by configuration bits as follows:
D5 = CNF13
D4 = CNF12
D3 = CNF11
D2 = CNF10
D1 = CNF09
D0 = CNF08

TABLE 24-5. HOST INTERFACE, BLOCK 0 INDEX 01

D1	D0	HOST INTERFACE
1	1	PCI bus
1	0	VL-bus/486-bus
0	1	Reserved
0	0	AT bus

D2	MULTIPLEXED HOST ADDRESS/ DATA BUS*
1	Demultiplexed host address/data bus
0	Multiplexed host address/data bus

NOTE:
Available for multiplexed VL-Bus or PCI bus only.

D3	VIDEO PORT / VAFC CONNECTOR
1	16-bit video connector, no VAFC connector
0	8-bit video connector/VAFC connector

D4	BURST MODE DISABLE
1	Burst mode enabled
0	Burst mode disabled

D5	ZERO WAIT STATE DISABLE
1	Zero wait state disabled
0	Zero wait state enabled

D6	AT BUS 16-BIT INTERFACE
1	AT bus interface is 16 bits
0	AT bus interface is 8 bits

D7	ENABLE VERTICAL RETRACE INTERRUPT
1	Vertical retrace interrupt enabled
0	Vertical retrace interrupt disable

NOTE:
The vertical retrace interrupt is enabled if selected by the VGA Vertical Sync End register and this bit is set to 1.

24.4 POWER-DOWN CONTROL

BITS	FUNCTION
D15:8	0000 0010 (index)
D7	Chip Active (Read-Only)
D6	Reserved (for testing)
D5:4	Chip Activity Time-out Period Select
D3:2	Monitor Power-down Control
D1	Chip Power-down Enable
D0	Chip Activity Time-out enable

NOTES:
(1) Bits D5:1 are reset at power-on and reset.
(2) Bit D7 is set at power-on by configuration bit CNF14.

TABLE 24-6. POWER-DOWN CONTROL, BLOCK 0 INDEX 02

D0	CHIP ACTIVITY TIMEOUT ENABLE
1	Enable
0	Disable (Default)

NOTE:
This bit is preset to 1. The bit state may change automatically when other registers are accessed.

D1	CHIP POWER-DOWN ENABLE
1	Enable
0	Disable (Default)

NOTE:
This bit is reset at power-on and reset.

D3	D2	MONITOR POWER-DOWN CONTROL
1	1	Monitor off: both HSYNC and VSYNC inactive
1	0	Monitor suspend: VSYNC inactive
0	1	Monitor stand-by: HSYNC inactive
0	0	Monitor on: both HSYNC and VSYNC active

NOTES:
(1) These values correspond to the VESA DPMS proposal
(2) These bits are reset at power-on and reset.

D5	D4	CHIP ACTIVITY TIMEOUT PERIOD SELECT
1	1	Time-out Period = Base Period times 4
1	0	Time-out Period = Base Period times 2
0	1	Time-out Period = Base Period times 1
0	0	Time-out Period = Base Period times 8

NOTES
(1) These bits are reset at power-on and reset.
(2) Where the Base Period = Vsync Period * 2^{15}

D7	CHIP ACTIVE
1	Chip responds normally to System Command(2)
0	Chip does not respond to any System Command(3)

NOTES:
(1) Bit D7 is read-only.
(2) This is the power-on setting when the chip active configuration bit is set high during power-on and reset.
(3) This is the power-on setting when the chip active configuration bit is set low during power-on and reset.

24.5 DISPLAY MEMORY INTERFACE

BITS	FUNCTION
D15:8	0000 0011 (index)
D7:5	Reserved
D4	Display memory multiple CAS/WE
D3:2	Display memory CAD width
D1:0	Reserved

NOTE:
Bits D7:2 are set at power-on by configuration bits as follows:
D4 = CNF54
D3 = CNF35
D2 = CNF34

TABLE 24-7. DISPLAY MEMORY CONFIGURATION - PART 1, BLOCK 0 INDEX 03

BITS	FUNCTION
D15:8	0000 0100 (index)
D7	Display memory refresh type
D6, D5	DRAM Refresh/Display Line
D4, D3	Reserved
D2	Display memory bus width
D1:0	Display memory RAS banks

NOTE:
Bits D7 and D2:0 are set at power-on by configuration bits as follows:
D7 = CNF55
D2 = CNF42
D1 = CNF41
D0 = CNF40

TABLE 24-8. DISPLAY MEMORY CONFIGURATION - PART 2, BLOCK 0 INDEX 04

D4	DISPLAY MEMORY MULTIPLE CAS/WE
1	Display memory chips use 1-CAS, multiple-WE
0	Display memory chips use multiple-CAS, 1-WE

D7	DISPLAY MEMORY REFRESH TYPE
1	Display memory refreshed using RAS-only refresh
0	Display memory refreshed using CAS-before-RAS refresh

D3	D2	DISPLAY MEMORY CAD WIDTH
1	1	Reserved
1	0	Display memory chips have 10 CAD inputs
0	1	Display memory chips have 9 CAD inputs
0	0	Display memory chips have 8 CAD inputs

D6	D5	DRAM REFRESH/DISPLAY LINE
0	x	3/5 DRAM Refresh
1	0	2 DRAM Refresh
1	1	1 DRAM Refresh

NOTE:
Sets the number of DRAM refresh cycles per display line.

D2	DISPLAY MEMORY BUS WIDTH
1	Display memory bus is 64 bits parallel
0	Display memory bus is 32 bits parallel

D1	D0	DISPLAY MEMORY RAS BANKS
1	1	Display memory has 2 RAS banks of 2M bytes each
1	0	Display memory has 2 RAS banks of 1M byte each
0	1	Display memory has 2 RAS banks of 512k bytes each
0	0	Display memory has a single RAS bank

BITS	FUNCTION
D15:8	0000 0101 (index)
D7	Not Used
D6	EDO Enable
D5	RMW timing
D4:3	CAS cycle timing
D2:1	RAS high-to-low timing
D0	RAS pre-charge timing

NOTE:
Bits D6:0 are set at power-on by configuration bits as follows:

D6 = CNF53
D5 = CNF52
D4 = CNF51
D3 = CNF50
D2 = CNF49
D1 = CNF48
D0 = CNF47

TABLE 24-9. DISPLAY MEMORY CONFIGURATION - PART 3, BLOCK 0 INDEX 05

D6	EDO ENABLE
1	EDO Memory Enable
0	EDO Memory Disable

D5	RMW TIMING
1	RMW requires one extra cycle between read and write
0	RMW performed by read and write back-to-back

D4	D3	CAS CYCLE TIMING
1	1	1 + (2~4ns) low; 1 - (2~4ns) high
1	0	1 MCLK low; 1 MCLK high
0	1	2 + (2~4) MCLK low; 2 - (2~4) MCLK high
0	0	2 MCLK low; 2 MCLK high

D2	D1	RAS HIGH-TO-LOW TIMING
1	1	0 MCLK High 2 MCLKs Low
1	0	3~7ns high; 4 MCLKs - (3~7ns) low
0	1	1 MCLK high; 3 MCLKs low
0	0	0 MCLKs high; 4 MCLKs low

D0	RAS PRE-CHARGE TIMING
1	RAS pre-charge time is 2 MCLKs
0	RAS pre-charge time is 4 MCLKs

24.6 RAMDAC INTERFACE

BITS	FUNCTION
D15:8	0000 0110 (index)
D7	Internal RAMDAC DAC off
D6	Local/external RAMDAC pulse width
D5	Local/external RAMDAC extra pin
D4	Reserved
D3:2	RAMDAC shadowing
D1	Internal RAMDAC
D0	External RAMDAC location

NOTES:
(1) Bits D5 and D3:2 are reset at power-on and reset.
(2) Bits D7:5 and D1 0 are set at power-on by configuration bits as follows:
D7 = CNF06
D6 = CNF07
D1 = CNF06
D0 = CNF05
(3) Configuration bit CNF06 is shared by bits D1 and D7. If the RAMDAC Location is configured as interna RAMDAC DAC Off is configured as enabled otherwise, it is configured as disabled

TABLE 24-10. RAMDAC INTERFACE, BLOCK 0 INDEX 06

D7	INTERNAL RAMDAC DAC OFF
1	RAMDAC interna DACs are disabled, drive zero current(1,2)
0	RAMDAC internal DACs are enabled(3)

NOTE:
(1) Selecting externa RAMDAC (setting bit D7 to 1) forces bit D1 to 0
(2) This is the power on setting when the chip active configuration bit is set high during power-on and reset
(3) This is the power-on setting when the chip active configuration bit is set low during power-on and reset

D6	LOCAL/EXTERNAL RAMDAC PULSE WIDTH (INTERNAL RAMDAC)
1	RAMDAC read/write pulse width is 16 MCLKs (20 MCLKs/LCKS)
0	RAMDAC read/write pulse width is 9 MCLKs (12 MCLKs/LCKS)

D5	LOCAL/EXTERNAL RAMDAC EXTRA PIN
1	Drive VIDS high within MM window, low otherwise
0	Drive VIDS low

D3	D2	RAMDAC SHADOWING
1	1	Write shadowing: Only RAMDAC writes performed; LDEV- not asserted for any cycles
1	0	Remote shadowing: RAMDAC reads and writes performed; LDEV- asserted for reads only(*)
0	1	Map out: ignore all RAMDAC port accesses
0	0	No shadowing: RAMDAC reads and writes performed; LDEV- asserted for reads and writes

NOTE:
*Enabling PCI palette snooping forces this mode.

D1	INTERNAL RAMDAC
1	Internal RAMDAC
0	External RAMDAC

NOTE:
Bit D1 is forced to 0 when bit D7 is set to 1.

D0	EXTERNAL RAMDAC LOCATION
1	Local: RAMDAC is on local bus
0	External: RAMDAC is on AT bus (Not supported in VL-Bus or PCI Bus.)

24.7 MONITOR AND VAFC CONNECTOR

The VAFC Connector Interface register specifies the functionality of the three VAFC connector pins. These pins can be used to permit an external device to share an external RAMDAC or use the internal RAMDAC by tri-stating certain WD9710 pins.

When enabled for input, each of the VAFC connector pins, when low, causes one or more WD9710 outputs to be tri-stated. When the internal RAMDAC is in use, tri-stated signals are driven from external devices into the internal RAMDAC. The EXSYNC pin controls the VSYNC, HSYNC, and BLANK outputs. The EXPCLK pin controls the PCLK output. The EXVID pin controls the VID bus.

When not used for feature connector control, these pins are available as general purposes I/O pins.

NOTE

The WD9710 also supports a standard 8-bit feature connector as a subset of the VESA Advanced feature connector. Refer to Section 5 for connection information.

The External Data Format field specifies the format of pixel data sent to an external RAMDAC as well as the format of pixel data received through the VAFC connector to the internal RAMDAC.

BITS	FUNCTION
D15:8	0000 0111 (index)
D7	External data format
D6	Single pin control
D5:4	EXVID pin control
D3:2	EXPCLK pin control
D1:0	EXSYNC pin control

TABLE 24-11. VAFC CONNECTOR INTERFACE, BLOCK 0 INDEX 07

Dx	Dy	EXSYNC/EXPCLK/EXVID PIN CONTROL
1	1	Ignore pin level and drive output high
1	0	Ignore pin level and drive output low
0	1	Pin may tri-state corresponding output pins
0	0	Ignore pin level and tri-state output

NOTES:

(1) The x indicates 1, 3, or 5 depending on the signal being EXSYNC, EXPCLK, or EXVID, respectively.

(2) The y indicates 0, 2, or 4 depending on the signal being EXSYNC, EXPCLK, or EXVID, respectively.

D6	SINGLE PIN CONTROL
1	EXSYNC pin controls, sync, BLANK, PCLK, and VID pins
0	Single pin control disabled

D7	EXTERNAL DATA FORMAT
1	External video data is 5-5-5 direct format, low byte first
0	External video data is 24-bit true color (RGB format - RG portion followed by B and then don't care)

BITS	FUNCTION
D15:8	0000 1000 (index)
D7:6	Not Used
D5:4	Composite sync control (see port 3?A bit 3)
D3:2	VSYNC polarity control (see port 3C2 bit 7)
D1:0	HSYNC polarity control (see port 3C2 bit 6)

TABLE 24-12. MONITOR INTERFACE, BLOCK 0 INDEX 08

D1	D0	CONTROL
1	1	Ignore VGA register bit and force value to 1*
1	0	Ignore VGA register bit and force value to 0(1)
0	X	Use value in VGA register

NOTE:
*Register bits still read back the value written.

BITS	FUNCTION
D15:8	0000 1001 (index)
D7	PCI Response Timing
D6:2	Not Used
D1	Interlaced mode
D0	Inverted LCLK

NOTES:
(1) Bit D0 is set at power-on by configuration bit CNF32.
(2) Bit D1 is reset at power-on and reset.
(3) Bit D7 is set at power-on by configuration bit CNF20.

TABLE 24-13. INTERLACE CONTROL, BLOCK 0 INDEX 09

D7	PCI RESPONSE TIMING
1	Medium Timing
0	Fast Timing

D1	INTERLACED MODE
1	Output to monitor is interlaced
0	Output to monitor is non-interlaced

24.8 MEMORY AND I/O RE-MAPPING

Many I/O locations can be re-mapped into memory or other I/O locations. This re-mapping is controlled by the I/O Re-mapping register, as follows:

BITS	FUNCTION
D15:8	0000 1010 (index)
D7:6	Remap 46E8
D5:4	Remap all 23CX ports
D3:2	Remap Location
D1	Remap host BLIT port (23C4/7h)
D0	Remap register access port 23C0/3h

NOTES:
1. Bits D3:0 are reset at power-on and reset.
2. Bits D7:4 are set at power-on by configuration bits as follows:
   D7 = CNF19
   D6 = CNF18
   D5 = CNF17
   D4 = CNF16

TABLE 24-14. I/O RE-MAPPING, BLOCK 0 INDEX 0A

D7	D6	REMAP 46E8
1	1	AT Mode Setup register is at 46EB
1	0	AT Mode Setup register is at 46EA
0	1	AT Mode Setup register is at 46E9
0	0	AT Mode Setup register is at 46E8

D5	D4	REMAP ALL 23CX PORTS
1	1	Ports are at E3CX
1	0	Ports are at A3CX
0	1	Ports are at 63CX
0	0	Ports are at 23CX (default)

D3	D2	REMAP LOCATION	
		23C0/3h	23C4/7h
1	1	Reserved	Reserved
1	0	B8000 - B9FFF	A0000 - AFFFF
0	1	A8000 - AFFFF	A0000 - A7FFF
0	0	B8000 - B9FFF	BA000 - BBFFF

D1	REMAP HOST BLIT PORT 23C4/7H
1	Host BLIT port is also at all doubleword memory locations in the range selected by bits 3:2.
0	Host BLIT port is at I/O locations 23C4/7

NOTE:
The I/O location of this port can be re-mapped via bit D5:4.

D0	REMAP REGISTER ACCESS PORT 23C0/3H
1	Register access port is also at all doubleword memory locations in the range selected by bits 3:2.
0	Register access port is at I/O locations 23C0/3

NOTE:
The I/O location of this port can be re-mapped via bit D5:4.

24.9 VGA REGISTER LOCK AND CHANGE

BITS	FUNCTION
D15 8	0000 1011 (index)
D7 4	Not Used
D3	Lock VGA CRT controller registers (port 3?5h)
D2	Lock VGA sequencer registers (port 3C5h)
D1	Lock VGA attribute controller registers (port 3C1h)
D0	Lock VGA graphics controller registers (port 3CFh)

TABLE 24-15. VGA LOCK CONTROL, BLOCK 0 INDEX 0B

Dn	LOCK VGA REGISTERS
1	Register bit is locked and cannot be written
0	Register bit is not locked

NOTE:
The Dn indicates any of bits D3:0 and its associated VGA registers listed in Table 24-15.

BITS	FUNCTION
D15:8	0000 1100 (index)
D7:5	Not Used
D4	Force CRTC 0-7 unlocked (see 3?5 index 11 bit 7)
D3	Force 3-cycle DRAM refresh (see 3?5 index 11 bit 6)
D2	Force graphics mode (see 3CF index 6 bit 0 and 3C0 index 10 bit 0)
D1	Force PCLK=VCLK (see 3C5 index 1 bit 3)
D0	Force 8-dot alpha mode (see 3C5 index 1 bit 0)

TABLE 24-16. VGA OVERRIDE CONTROL, BLOCK 0 INDEX 0C

D4	FORCE CRTC 0-7 UNLOCKED
1	CRTC registers 0-7 cannot be locked by 3?5.11 bit 7
0	CRTC registers 0-7 may be locked or unlocked, per 3?5.11 bit 7

D3	FORCE 3-CYCLE DRAM REFRESH
1	DRAM refresh is always 3-cycle
0	DRAM refresh may be 3-cycle or 5-cycle, per 3?5.11 bit 6

D2	FORCE GRAPHICS MODE
1	Display is always in graphics mode
0	Display may be alpha or graphics mode, per 3CF.5 bit 0 and 3C0.10 bit 0

D1	FORCE PCLK = VCLK
1	PCLK is always VCLK*
0	PCLK may be VCLK or VCLK/2, per 3C5.1 bit 3
NOTE: *PCLK can also be MCLK	

D0	FORCE 8-DOT ALPHA MODE
1	Alpha mode is always 8-dot
0	Alpha mode may be 8-dot or 9-dot, per 3C5.1 bit 0

BITS	FUNCTION
D15:8	0000 1101 (index)
D7:3	Not Used
D4	Disable VGA attribute controller palette
D3	Correct VGA 9-dot underline
D2	Disable dynamic refresh
D1	Disable VGA border
D0	Disabled VGA cursor blink

TABLE 24-17. VGA DISABLE CONTROL, BLOCK 0 INDEX 0D

D4	DISABLE VGA ATTRIBUTE CONTROLLER PALETTE
1	Attribute controller palette is bypassed in all modes
0	Pixels are translated through attribute controller palette in certain modes

D3	CORRECT VGA 9-DOT UNDERLINE
1	Cursor and underline in 9-dot are 9 dots wide
0	Cursor and underline in 9-dot are only 8 dots wide

D2	DISABLE DYNAMIC REFRESH
1	DRAM refresh disabled*
0	DRAM refresh enabled
NOTE: *This bit should be used during debug only, as it may result in corruption of display memory contents.	

D1	DISABLE VGA BORDER
1	VGA border disabled
0	VGA border enabled

D0	DISABLED VGA CURSOR BLINK
1	VGA text cursor blink disabled
0	VGA text cursor blink enabled

24.10 MASTER PIN CONTROL

BITS	FUNCTION
D15:8	0000 1110 (index)
D7:6	Not Used
D5	Tri-state EABUF, BUFDIR, EDBUF
D4	Tri-state EBROM
D3	Tri-state MD63:32
D2	Tri-state MD31:0
D1	Tri-state RAS1:0, CAS7:0, WE1:0, TR/OE1:0
D0	Tri-state MA9:0

TABLE 24-18. TRI-STATE CONTROL - PART 1, BLOCK 0 INDEX 0E

BITS	FUNCTION
D15:8	0000 1111 (index)
D7	Tri-state MVVSYNC, MVHSYNC
D6	Tri-state MVD7:0
D5	Tri-state PCLK
D4	Tri-state VID7:0, VIDS
D3	Tri-state WCLK
D2	Tri-state RPLT, WPLT
D1	Tri-state EXVSYNC, EXHSYNC, EXPCLK
D0	Tri-state HSYNC, VSYNC, BLANK

TABLE 24-19. TRI-STATE CONTROL - PART 2, BLOCK 0 INDEX 0F

Dn	TRI-STATE
1	Tri-state pin or group of pins
0	Do not tri-state pin (unless specified elsewhere)

NOTE:
The Dn indicates any of bits D7:0 and their associated function as listed in Table 24-19.

24.11 DISPLAY MEMORY MAPPING

BITS	FUNCTION
D15:12	0001 0000 (index)
D7	Enable Alternate Wake-up Register 3C3h
D6	Disable VGA I/O addresses
D5:4	Linear display memory aperture
D3	Configuration read enable
D2	Reserved
D1	Enable linear address space
D0	Disable VGA address space

NOTES:
(1) Bits D6, D3, and D1:0 are reset at power-on and reset.
(2) Bit D7 is set at power-on by configuration bit CNF15.

TABLE 24-20. DISPLAY MEMORY APERTURE, BLOCK 0 INDEX 10

D6	DISABLE VGA I/O ADDRESSES
1	VGA I/O addresses do not respond
0	VGA I/O addresses respond

NOTES:
When this bit is set to 1, it works with bits D0 and D1 to control display memory access.

D5	D4	LINEAR DISPLAY MEMORY APERTURE
1	1	Reserved
1	0	Linear display memory aperture is 4M bytes
0	1	Linear display memory aperture is 2M bytes
0	0	Linear display memory aperture is 1M byte

D3	CONFIGURATION READ ENABLE
1	Reads to display memory space return configuration bit data
0	Reads to display memory space return display memory data

D1	ENABLE LINEAR ADDRESS SPACE
1	Display memory can be accessed at linear addresses above 1M(1,2)
0	Display memory cannot be accessed at linear addresses above 1M

NOTES:
When this bit is set to 1, it works with bits D0 and D6 to control display memory access.

D0	DISABLE VGA ADDRESS SPACE
1	Display memory cannot be accessed at VGA addresses
0	Display memory may be accessed at VGA addresses

D0	DISABLE VGA ADDRESS SPACE

NOTES:

(1) When this bit is set to 0 and bit D1 is set to 1, access is available to display memory through both address spaces simultaneously

(2) When this bit is set to 1 and bits D1 and D6 are also set to 1, the WD9710 can be removed from the VGA memory and I/O space entirely, permitting a second VGA controller in the system to operate at these locations while the WD9710 operates at upper memory address and extended I/O address locations.

BITS	FUNCTION
D15:8	0001 0001 (index)
D7:0	Display memory linear start address

TABLE 24-21. DISPLAY MEMORY LINEAR START ADDRESS, BLOCK 0 INDEX 11

The Display Memory Linear Start Address register specifies the CPU address at the beginning of display memory when linear addressing is specified by the display memory start address of the Display Memory Aperture register. The value in this register specifies the starting address in megabytes. This address must be aligned to whatever aperture is specified.

24.12 ROM INTERFACE REGISTER

BITS	FUNCTION
D15:8	0001 0010 (index)
D7:6	Lower 2 bits of the Display Memory Linear Start Address
D5	Enable ROM Base Address (PCI Host Only)
D4	ROM timing
D3	ROM external select
D2	ROM Aperture B
D1	ROM Aperture A
D0	Map out BIOS ROM

NOTES:

(1) Bit D5 is read/only.

(2) Bits D5:3 and D0 are set at power-on by configuration bits as follows:
D5 = CNF21
D4 = CNF27
D3 = CNF26
D0 = CNF24

TABLE 24-22. ROM INTERFACE REGISTER, BLOCK 0 INDEX 12

D7:6	LOWER 2 BITS OF DISPLAY MEMORY LINEAR START ADDRESS
D7	Bit 0 of Display Memory Linear Start Address
D6	Bit 1 of Display Memory Linear Start Address

D5	ENABLE ROM BASE ADDRESS
1	ROM Base Address Enabled (PCI Host Only)
0	ROM Base Address Disabled

D4	ROM TIMING
1	ROM cycle is 4 MCLKs
0	ROM cycle is 8 MCLKs

D3	ROM EXTERNAL SELECT
1	External ROM - ROM address is sent from host, ROM drives host bus directly, generate EBROM- only (Not supported by PCI Bus.)
0	Local ROM - ROM address sent through MD31:16, ROM data is read through MD7:0

D2	ROM APERTURE B
0	ROM is not available at A000:0
1	ROM (64k bytes) is also available at A000:0-AFFF:F)

D1	ROM APERTURE A
0	ROM is 32k bytes (C000:0-C7FF:F)
1	ROM is 64k bytes (C000:0-CFFF:F)

D0	MAP OUT BIOS ROM
0	ROM can be read at C000:0
1	ROM is mapped out

24.13 VIDEO FIFO CONTROL

BITS	FUNCTION
D15:8	0001 0011 (index)
D7:4	Stretch FIFO Request Point
D3:0	Video FIFO request point

NOTE:
Bits D3:0 are set at power-on by configuration bits as follows:

D3 = CNF31
D2 = CNF30
D1 = CNF29
D0 = CNF28

TABLE 24-23. VIDEO FIFO CONTROL, BLOCK 0 INDEX 13

D3:0	VIDEO FIFO REQUEST POINT(1)
n	2n + 1

NOTES:
(1) When the number of FIFO's entry is empty.
(2) Bits D3:0 are set at power-on by configuration bits.

D7:4	STRETCH FIFO REQUEST POINT(1)
m	2m + 1

NOTES:
(1) When the number of FIFO's entry is empty.
(2) Bits D7:4 are set to 0100b.

24.14 COMPANION CHIP INTERFACE

BITS	FUNCTION
D15:8	0001 0100 (index)
D7:4	Not Used
D3	Enable Co-processor
D2	CLK divided by 2 for VAFC
D1	VAFC Disable
D0	Reserved

TABLE 24-24. COMPANION CHIP INTERFACE, BLOCK 0 INDEX 14

D3	ENABLE COPROCESSOR
1	Co-processor Control Enabled on FPUSR3 and FPUSR4 (pins 159 and 158, respectively)
0	Co-processor Control Disabled

D2	CLK DIVIDED BY 2 FOR VAFC
1	CLK Divided by 2
0	CLK Not Divided

D1	VAFC DISABLE
1	VAFC Disabled
0	VAFC Interface Enabled

24.15 USR PINS DEFINITION

BITS	FUNCTION
D15:D8	0001 0101
D7	Enable USR2:4}
D6	Enable USR1
D5	Enable USR0
D4	USR4 (Pin 158)
D3	USR3 (Pin 159)
D2	USR2 (Pin 164)
D1	USR1 (Pin 165)
D0	USR0 (Pin 166)

TABLE 24-25. USR PINS DEFINITION, BLOCK 0 INDEX 15

24.16 INTERRUPT STATUS REGISTER

Interrupt status information is available in the Interrupt Status register in the System Control Registers block. This registers returns information as to which part of the WD9710 caused an interrupt.

Reading this register automatically resets any interrupts returned except the VGA vertical interrupt, which is handled per the VGA specification.

Unassigned interrupts are returned as zeroes.

BITS	FUNCTION
D15:8	0000 0000 (index)
D7	Interrupt 7 active
⇓	⇓
D1	Interrupt 1 active
D0	Interrupt 0 active

TABLE 24-26. INTERRUPT STATUS, R/O BLOCK 1 INDEX 00

24.17 EXTENDED ADDRESS OFFSET REGISTERS

The Extended Address Offset A and B registers extend the Paradise PR0A and PR0B registers to 12 bits each. Writing the registers through these ports sets all twelve bits. Writing either register through the non-extended ports automatically resets the four high-order bits of both of these registers.

BITS	FUNCTION
D15:12	0000 (index)
D11:0	Primary address offset, in 4k byte chunks

TABLE 24-27. EXTENDED ADDRESS OFFSET A, BLOCK 2 INDEX 0

BITS	FUNCTION
D15:12	0001 (index)
D11:0	Alternate address offset, in 4k byte chunks

TABLE 24-28. EXTENDED ADDRESS OFFSET B, BLOCK 2 INDEX 1

24.18 DEVICE STATUS REGISTER

The Device Status register is a dedicated 16-bit read-only I/O register at location 23CC-D (which can be remapped per the I/O Re-mapping register). Reads to this register are always returned immediately without waiting for the command FIFO to empty. Writing this register may be used to abort a BITBLT in progress. The contents of this register are as follows:

BITS	FUNCTION
D15	Drawing operation status/abort
D14	Command queue full *r/o*
D13:12	Host BLIT status *r/o*
D11	Vertical display enable *r/o*
D10	Write Buffer Empty
D9:4	Register Block Pointer
D3:0	Command FIFO status *r/o*

TABLE 24-29. DEVICE STATUS, PORT 23CC/Dh

D15	DRAWING ENGINE STATUS/ABORT
1	Drawing engine operation in progress and/or command queue is not empty
0	No operation in progress and command queue is empty / abort drawing engine operation

D14	COMMAND QUEUE FULL
1	Command queue full
0	Command queue not full

D13	D12	HOST BLIT STATUS
1	1	Host BLIT read in progress
1	0	Host BLIT write in progress
0	X	No Host BLIT in progress

D11	VERTICAL DISPLAY ENABLE
1	Vertical blank is active
0	Vertical blank not active

D10	WRITE BUFFER EMPTY
1	Write Buffer is Empty
0	Write Buffer Not Empty

D9:4	REGISTER BLOCK POINTER
n	Block Pointer Value (D5:0) Read Only

D3	D2	D1	D0	COMMAND FIFO STATUS
1	1	1	1	One available entry in command FIFO
1	1	1	0	Two available entries in command FIFO
⇓				⇓
0	0	0	1	Seven entries available in command FIFO
0	0	0	0	Command FIFO is full

24.19 BI-ENDIAN SUPPORT

The WD9710 supports Bi-Endian operation on its PCI interface. This section describes the additional hardware needed to provide this support, which is built into the WD9710.

24.19.1 Linear Memory Aperture

The base address register located at 10h in the configuration space is expanded from 4M bytes to 8M bytes. The lower 4M bytes are little-Endian with no byte swapping. The upper 4M bytes are big-Endian. Both windows are active simultaneously. The WD9710 decides if the pixel data is big-Endian or little-Endian by looking at bit 22 of the address. For apertures of less than 4M bytes, the big-Endian and little-Endian apertures start at the bottom of each 4M byte boundary. The WD9710 supports 1M byte, 2M bytes, or 4M bytes of memory. Also, the video and graphics must be the same byte size in the big-Endian window. This area cannot be cached.

BASE ADDRESS REGISTER 10h																															
3	3	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1												
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
Read/Write																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Big Endian byte swapping is handled as follows:

Pixel Size	Register Setting (Block 11, Index 4 [4:2])	Source Bytes				Destination Bytes			
≤ 8 bits Note	000/001/010	3	2	1	0	3	2	1	0
15/16 bits	1000/101	3	2	1	0	2	3	0	1
≥ 24 bits	111	3	2	1	0	0	1	2	3
Note: Packed 24 is passed with no swapping.									

24.19.2 Input/Output

Hard decode and soft decode of VGA registers and memory are supported. The hard decode is like a conventional VGA device, claiming I/O locations 3B0h-3BBh, 3C0h-3CFh, 3D0h-3DFh (plus alias 23C0h-23C7h) and memory locations A0000h - BFFFFh. Locations 46E8h and 102h are not decoded when the WD9710 is configured as a PCI device. These I/O and memory locations are treated as little-Endian only. Re-mapping of registers, as defined in the specification, is still functional when set for hard decode.

Soft decode is used, all I/O register access is treated as memory mapped I/O. A 64k byte memory aperture is reserved for this purpose. The lower 32k bytes are treated as little-Endian and the upper 32k bytes are treated as big-Endian. The same address as the I/O register is decoded within each 32k byte memory space. Relocation of the 23Cxh ports is not permitted for soft decode operation. Also, palette snooping is not supported for soft decode operation. The VGA memory space (A0000h-BFFFFh) is not decoded.

Selection of decode the method is provided by a configuration register located at 40h in the configuration space. This bit is cleared at power-up and reset.

Bit 0	Function
0	Conventional VGA Hard Decode
1	I/O Space Moved to Re-locatable Memory Map

CONFIGURATION REGISTER 40h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	*

NOTE: Bit 0 is the Read/Write bit.

A base address register is provided at location 14h in the PCI configuration space for the soft decode address mapping. The 64k byte locations are reserved. This area cannot be cached.

CONFIGURATION REGISTER 14h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/Write																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Byte swapping is performed on register writes based on received size, except for BLT register 23C4h. For writes to this register, byte swapping is performed in the same manner that linear memory address mapping is performed on pixel data.

24. 19.2.1 Read-Only-Memory

ROM is always considered little-Endian.

24. 19.2.2 Wake-Up

The following commands are needed to wake up the WD9710 as a hard decoded Bi-Endian PCI VGA controller.

- Write configuration register 04h ≤ xxxFh (enable IO and memory)
- Write configuration register 10h ≤ linear memory base address
- Write configuration register 3Ch ≤ expansion ROM base address
- Initialize all WD9710 internal control registers via IO
- Write commands to standard and extended VGA register space.

The following commands are needed to wake up the WD9710 as a relocatable Bi-Endian PCI VGA controller:

- Write configuration register 04h ≤ xxxFh (enable IO and memory)
- Write configuration register 10h ≤ linear memory base address

- Write configuration register 14h ≤ control base address
- Write configuration register 3Ch ≤ expansion ROM base address
- Write configuration register 40h ≤ xxx1h
- Initialize all WD9710 internal control registers via memory
- Write commands to standard and extended VGA register space with offset of control base address.

24.19.3 Summary

Hard Decode (Configuration Register 40h, Bit 0 = 0):

- Reserve I/O addresses 3B0h-3BBh, 3C0h-3CFh, 3D0h-3DFh plus alias 23C0h-23C7h.
- Reserve A0000h - BFFFFh memory addresses.
- Keep all extended register control of the host interface.
- Little-Endian only.

Soft Decode (Configuration Register 40h, Bit 0 = 1):

- I/O moved to memory mapped I/O
- Same address retained within the 32k byte address space
- Disable palette snooping
- Disable original memory map of 23C0h and 23C4h.
- Release A0000h-BFFFFh memory addresses
- Lower 32k byte address is little-Endian
- Upper 32k byte address is big-Endian with byte swapping based on pixel size or register size. (BLT writes at address 23C4h)
- Uses the same format as memory swapping

Linear Memory Aperture:

- Reserves 8M bytes of memory.
- Inset window (video) and desktop (graphics) must be same byte size on big-Endian aperture
- Lower 4M bytes treated as little-Endian
- Upper 4M bytes treated as big-Endian
- Both apertures are active at the same time

Big-Endian Byte Swapping (Based on Block 11, Index 4, Bits 4:2):

- 1234 ≥ 4321 (24/32 bits per pixel)111
- 1234 ≥ 2143 (15/16 bits per pixel)100/101
- 1234 ≥ 1234 (8 or less bits per pixel)000/001/010

ROM is Always Considered Little-Endian.

25.0 GLOBAL RESOURCE MAP

25.1 EXTENDED REGISTERS PORT MAP

PORT	FUNCTION
23C0	Register Access (low byte)[1]
23C1	Register Access (high byte)[1]
23C2-3	Register Access (high word, 32-bit access)(1)
23C4-7	Host BLIT I/O (1)
23C8-9	Hardware Cursor Registers
23CA-B	Reserved
23CC-D	Status register

NOTES:
(1) These registers may be memory-mapped
(2) These registers also have dedicated pins

TABLE 25-1. EXTENDED REGISTERS PORT MAP

25.2 REGISTER BLOCK MAP

BLOCK POINTER	REGISTER ACCESS PORT ACCESSES
0-2	System Control registers
3	Hardware Clipping registers
4-5	BITBLT registers
7	Vector
9	Stretch Mode Registers
11	Serializer
12	Reserved
13	Reserved
14	Signature Analyzer registers
15	Reserved
16	Scratchpad registers (contains 8 registers)
17	Clock generator registers
30	VGA Attribute Controller registers (3C0/1)
31	VGA Sequencer registers (3C4/5)
32	VGA Graphics Controller registers (3CE/F)
33	VGA CRT Controller registers (3?4/5)
38	(reserved for testing)
3F	(reserved for context switching)

TABLE 25-2. REGISTER BLOCK MAP

TABLE 25-2. REGISTER BLOCK MAP (Continued)

25.3 GLOBAL INTERRUPT MAP

INTERRUPT	FUNCTION
0	VGA vertical interrupt
1	BITBLT/vector interrupt
2	Clipping interrupt
3	Motion Video Port interrupt
4	Signature analyzer interrupt

TABLE 25-3. GLOBAL INTERRUPT MAP

25.4 CONFIGURATION OPTIONS

The WD9710 is configured at power-on by pull-down resistors on the 64-bit MD bus. Any MD pin not pulled down by an external resistor is pulled up internally, resulting in a 1 being read. On reset, many of these bits are checked and the value causes one or more register bits to be set.

NOTE

A configuration pin with an external pull-down causes its corresponding register bit to be cleared to 0 during reset. A configuration pin without a pull-down causes the bit to be set to 1.

All of the registers set by configuration are available for inspection and change by the host.

The current state of all configuration bits (including unused ones) may be read by the host at any time by setting the Configuration Read Enable bit in the Display Memory Aperture register and reading the display memory at the active address. All 64 configuration bits will be returned in any aligned 64-bit memory space read. For example,

a word read to A000:0 might return configuration bits 15:0 and a word read to A000:2 might return bits 31:16.

NOTE

For configuration purposes, the MD lines (MD63:00) are referred to as configurations bits CNF63:00.

CNF BITS	CONFIGURATION FUNCTION
00	VCLK internal- / external+
01	MCLK internal- / external+
04:02	MCLK frequency select
05	External/Internal RAMDAC
06	Internal RAMDAC
07	RAMDAC pulse width
09:08	Host interface
10	Multiplexed host address/data
11	Video port / VAFC connector
12	Burst mode enable
13	Zero wait state disable
14	Chip Active
17:16	Remap all 23CXh ports
19:18	Remap 46E8h
20	PCI Response Timing
21	PCI Enable ROM Base Address
22:23	Reserved
24	Map out BIOS ROM
25	Reserved
26	ROM external select
27	ROM timing

TABLE 25-4. CONFIGURATION OPTIONS

CNF BITS	CONFIGURATION FUNCTION
31:28	Video FIFO request point
32	Inverted LCLK
33	VAFC Disable
35:34	Display memory CAD width
39:36	TRLCK to VLCK Clock Skew
41:40	Display memory RAS banks
42	Display memory bus width
46:43	MCLK to MDLCK Clock Skew
47	RAS pre-charge timing
49:48	RAS high-to-low timing
51:50	CAS cycle timing
52	RMW cycle timing
53	Enable EDO Memory
54	Display memory multiple CAS/WE
55	Display memory refresh type
63:56	Scratch register preset bits

TABLE 25-4. CONFIGURATION OPTIONS (Continued).

25.5 CONFIGURATION REGISTERS

The following table provides a list of the configuration bits, their register location, and function. The registers allow the configuration bits to be modified after start up or refresh. The table also references other tables where the register descriptions are located.

CONFIGURATION (CNF) BITS	REGISTER BLOCK/INDEX	REGISTER BITS	FUNCTION	REFERENCE TABLE
00[1]	17/00	D0	VCLK Source	14-2
		D2	VCLK Generator State	14-2
		D10	VCLK External Clock Load Enable	14-2
01	17/02	D0	MCLK Source	14-5
		D2	MCLK Generator State	14-5
04:02	17/02	D6:4	MCLK Frequency Select	14-5
05	00/06	D0	External RAMDAC Location	24-10
06[2]	00/06	D1	Internal RAMDAC	24-10
		D7	Internal RAMDAC DAC Off	24-10
07	00/06	D6	Local / External RAMDAC Pulse Width	24-10
09:08	00/01	D1:0	Host Interface	24-5
10	00/01	D2	Multiplexed Host Address / Data Bus	24-5
11	00/01	D3	Video Port / VAFC Connector	24-5
12	00/01	D4	Burst Mode Enable	24-5
13	00/01	D5	Zero Wait State Disable	24-5
14	00/02	D7	Chip Active	24-6
15	00/01	D7	Enable Wake-up Register 3C3h on VL-bus	24-20
17:16	00/0A	D5:4	Remap All 23Cxh Ports	24-14
19:18	00/0A	D7:6	Remap 46E8h	24-14
20	00/09	D7	PCI Response Timing	24-13
21	00/12	D5	Enable ROM Base Address (PCI Bus Only)	24-22
22, 23	Reserved	---	---	---
24	00/12	D0	Map Out BIOS ROM	24-22
25	Reserved	---	---	---
26	00/12	D3	ROM External Select	24-22
27	00/12	D4	ROM Timing	24-22
31:28	00/13	D3:0	Video FIFO Request Point	24-23
32	00/09	D0	Inverted LCLK	24-13
33	00/14	D1	VAFC Disable	24-24
35:34	00/03	D3:2	Display Memory CAD Width	24-7
39:36	17/05	D3:D0	TRLCK to VLCK Clock Skew	14-9

TABLE 25-5. CONFIGURATION BIT REGISTER LOCATIONS

CONFIGURATION (CNF) BITS	REGISTER BLOCK/INDEX	REGISTER BITS	FUNCTION	REFERENCE TABLE
41:40	00/04	D1:0	Display Memory $\overline{RAS}$ Banks	24-8
42	00/04	D2	Display Memory Bus Width	24-8
46:43	17/05	D7:D4	MCLK to MDLCK Clock Skew	14-9
47	00/05	D0	$\overline{RAS}$ Precharge Timing	24-9
49:48	00/05	D2:1	$\overline{RAS}$ High-to-Low Timing	24-9
51:50	00/05	D4:3	$\overline{CAS}$ Cycle Timing	24-9
52	00/05	D5	RMW Timing	24-9
53	00/05	D6	EDO Enable	24-9
54	00/03	D4	Display Memory Multiple $\overline{CAS}$ / WE	24-7
55	00/04	D7	Display Memory Refresh Type	24-8
63:56	16/nn:00	D7:0 (at each index)	Scratchpad Registers	21-1

NOTE

(1) Configuration bit CNF0 is shared by register bits D0, D2, and D10.

(2) Configuration bit CNF6 is shared by register bits D1 and D7. If the RAMDAC location is configured as internal, RAMDAC DAC Off is configured as enabled. Otherwise, it is disabled.

TABLE 25-5. CONFIGURATION BIT REGISTER LOCATIONS

26.0 DISPLAY MEMORY FORMATS

The section provides the following tables that describe display memory formats:

- Table 26-1 provides Display Memory Layout Formats.
- Table 26-2 provides Display Memory Pixel Formats
- Table 26-3 provides Display Memory YUV Formats

These tables provide reference information for designers who want to know how the WD9710 memory is formatted, but otherwise this information is transparent to users.

26.1 DISPLAY MEMORY LAYOUT FORMATS

Table 26-1 lists the display memory layout formats. Each memory mode is listed as 16 or 24 bytes in 8 or 16 byte segments. Offset byte 0 points to the first segment of either 8 or 16 bytes, offset byte 8 points to the second segment of 8 or 16 bytes, and offset byte 16 points to the third segment (for 24-byte modes only) of 8 bytes. Each byte contains a specific data type depending on its location and the selected mode. The data types are described in the legend at the end of the table.

OFFSET BYTE	MODE	0	1	2	3	4	5	6	7
---	T[1]	*STANDARD VGA TEXT MODE, 256 CHARACTERS*							
0	---	Ch0	A0	F00	X	Ch1	A1	F01	X
8	---	Ch2	A2	F02	X	---	---	---	---
---	*V*[1]	*STANDARD VGA 1, 2, AND 4 BIT PLANAR MODES*							
0	---	V0/7^{P}	---	---	V0/7^{P}	V8/15	---	---	V8/15
8	---	V16/23	---	---	V16/23	---	---	---	---
---	*V2*[1]	*STANDARD VGA 2 BIT PACKED MODE (4 COLOR)*							
0	---	V0/3	V4/7	X	X	V8/11	V12/15	X	X
8	---	V16/19	---	---	---	---	---	---	---
---	*8*	*DESKTOP 8 BIT (256 COLOR)*							
0	---	V0	V1	V2	V3	V4	V5	V6	V7
8	---	V8	---	---	---	---	---	---	---
---	*15*	*DESKTOP 15 BIT (32K COLOR)*							
0	---	V0^{L}	V0^{H}	V1	V1	V2	V2	V3	V3
8	---	V4	V4	---	---	---	---	---	---
---	*16*	*DESKTOP 16 BIT (64K COLOR)*							
0	---	V0^{L}	V0^{H}	V1	V1	V2	V2	V3	V3
8	---	V4	V4	---	---	---	---	---	---
---	*24*[1]	*DESKTOP 24 BIT (16M COLOR), PACKED 24*							
0	---	V0^{B}	V0^{G}	V0^{R}	V1	V1	V1	V2	V2
8	---	V2	V3	V3	V3	---	---	---	---
---	*32*	*DESKTOP 24 BIT (16M COLOR), 1 UNUSED BYTE*							
0	---	V0^{B}	V0^{G}	V0^{R}	X	V1	V1	V1	X
8	---	V2	V2	V2	X	---	---	---	---

TABLE 26-1. DISPLAY MEMORY LAYOUT FORMATS

OFFSET BYTE	MODE	0	1	2	3	4	5	6	7
---	*8/8*	*DESKTOP 8 BIT, INSET 8 BIT, SHARED MEMORY, NO OCCLUSION*							
0	---	V0	V1	V2	V3	V4	V5	V6	V7
---	---	M0	M1	M2	M3	M4	M5	M6	M7
8	---	V8	---	---	---	---	---	---	---
---	---	M8	---	---	---	---	---	---	---
---	*15/8*	*DESKTOP 15 BIT, INSET 8 BIT, SHARED MEMORY*							
0	---	$V0^{L}$	$V0^{H15}$	V1	V1	V2	V2	V3	V3
	---	M0	$K0^{7}$	M1	K1	M2	K2	M3	K3
8	---	V4	V4	---	---	---	---	---	---
---	---	M4	K4	---	---	---	---	---	---
---	*15/12*	*DESKTOP 15 BIT, INSERT 12 BIT (YUV 4:1:1), SHARED MEMORY*							
0	---	$V0^{L}$	$V0^{H15}$	V1	V1	V2	V2	V3	V3
---	---	$M0^{L}$	$M0^{H1}$	M1	M1	M2	M2	M3	M3
8	---	V4	V4	---	---	---	---	---	---
---	---	M4	M4	---	---	---	---	---	---
NOTE: *Bits 14:12 = don't care.*									
---	*16/16*	*DESKTOP 16 BIT, INSET 16 BIT, SHARED MEMORY, NO OCCLUSION*							
0	---	$V0^{L}$	$V0^{H}$	V1	V1	V2	V2	V3	V3
---	---	$M0^{L}$	$M0^{H}$	M1	M1	M2	M2	M3	M3
8	---	V4	V4	---	---	---	---	---	---
---	---	M4	M4	---	---	---	---	---	---
---	*32/16*	*DESKTOP 24 BIT, INSET 16 BIT, SHARED MEMORY*							
0	---	$V0^{B}$	$V0^{G}$	$V0^{R}$	$K0^{7}$	V1	V1	V1	K1
---	---	M0L	M0H15	X	X	M1	M1	X	---
8	---	V2	V2	V2	K2	---	---	---	---
---	---	M2	M2		---	---	---	---	---
---	*8+8*	*DESKTOP 8 BIT, INSET 8 BIT, SEPARATE MEMORY*							
0	---	$V0^{C}$	V1	V2	V3	V4	V5	V6	V7
8	---	M0	M1	M2	M3	M4	M5	M6	M7
16	---	V8	---	---	---	---	---	---	---
---	*15+16*	*DESKTOP 15 BIT, INSET 16 BIT, SEPARATE MEMORY*							
0	---	$V0^{L}$	$V0^{H15}$	V1	V1	V2	V2	V3	V3
8	---	$M0^{L}$	$M0^{H}$	M1	M1	M2	M2	M3	M3
16	---	V4	V4	---	---	---	---	---	---
---	*16+16*	*DESKTOP 16 BIT, INSET 16 BIT, SEPARATE MEMORY*							
0	---	$V0^{L}$	$V0^{HC}$	V1	V1	V2	V2	V3	V3
8	---	$M0^{L}$	$M0^{H}$	M1	M1	M2	M2	M3	M3
16	---	V4	V4	---	---	---	---	---	---

TABLE 26-1. DISPLAY MEMORY LAYOUT FORMATS (Continued)

OFFSET BYTE	MODE	0	1	2	3	4	5	6	7
S/I	8s16	DESKTOP 8 BIT (256 COLOR), INSET 16 BIT, STRETCH MODE (DESKTOP DATA)							
0	---	V0	V1	V2	V3	V4	V5	V6	V7
8	---	V8	---	---	---	---	---	---	---
S/I	8s16	*DESKTOP 8 BIT (256 COLOR), INSET 16 BIT, STRETCH MODE (INSET DATA)*							
0	---	$M0^L$	$M0^H$	M1	M1	M2	M2	M3	M3
8	---	$M4^L$	$M4^H$	---	---	---	---	---	---
S/I	15s16	*DESKTOP 15 BIT (32K COLOR), INSET 16 BIT, STRETCH MODE (DESKTOP DATA)*							
0	---	$V0^L$	$V0^H$	V1	V1	V2	V2	V3	V3
8	---	V4	V4	---	---	---	---	---	---
S/I	15s16	*DESKTOP 15 BIT (32K COLOR), INSET 16 BIT, STRETCH MODE (INSET DATA)*							
0	---	$M0^L$	$M0^H$	M1	M1	M2	M2	M3	M3
8	---	$M4^L$	$M4^H$	---	---	---	---	---	---
S/I	16s16	*DESKTOP 16 BIT (64K COLOR), INSET 16 BIT, STRETCH MODE (DESKTOP DATA)*							
0	---	$V0^L$	$V0^H$	V1	V1	V2	V2	V3	V3
8	---	V4	V4	---	---	---	---	---	---
S/I	16s16	*DESKTOP 16 BIT (64K COLOR), INSET 16 BIT, STRETCH MODE (INSET DATA)*							
0	---	$M0^L$	$M0^H$	M1	M1	M2	M2	M3	M3
8	---	$M4^L$	$M4^H$	---	---	---	---	---	---

LEGEND:

[1] Limited acceleration in these modes

[7] Bit 7 of this pixel selects between VGA (0) and Multimedia (1)

[15] Bit 15 of this pixel selects between VGA (0) and Multimedia (1)

A = Character Attribute byte

B = Blue byte of 24-bit RGB pixel

C = Chromakey color selects between VGA and Multimedia

Ch = ASCII Character byte

F = Character Font byte

G = Green byte of 24-bit RGB pixel

H = High byte of 15- or 16-bit pixel

K = Chromakey byte

L = Low byte of 15- or 16-bit pixel

M = Low nibble of this byte

N = High nibble of this byte

P = Pixels are planar, each pixel appears in all four bytes

R = Red byte of 24-bit RGB pixel

S/I = Scaling and Interpolation (stretch) mode

a. In S/I mode, the desktop data offset byte is from the starting address defined by 'start address high' and 'start address low' in the CRT register block (Port 3?5h Index C and D).

b. In S/I mode, the inset data offset byte is from the starting address defined by 'motion video source data start address high' and 'motion video source data start address low' in the Stretch register block (Block 9, Index 1 and 0).

V = VGA graphics

X = Don't care

TABLE 26-1. DISPLAY MEMORY LAYOUT FORMATS (Continued)

26.2 DISPLAY MEMORY PIXEL FORMATS

The display memory pixel formats are listed in Table 26-2.

BITS	FUNCTION
V4: 4-BIT PLANAR (16-COLOR)	
D31,23,15,7	Left-most pixel, planes 3:0
D30,22,14,6	Second Pixel
⇓	⇓
D24,16,8,0	Right-most pixel
	display eight pixels, left to right
V2: 2-BIT PLANAR (4-COLOR)	
D31:24	XXXX XXXX
D23,7	Left-most pixel, planes 1:0
D22,6	Second Pixel
⇓	⇓
D16,0	Right-most pixel
D15:8	XXXX XXXX
	display eight pixels, left to right
V2B: 2-BIT PACKED (4-COLOR)	
D31:24	XXXX XXXX
D23:16	XXXX XXXX
D15:8	XXXX XXXX
D7:6	Left-most pixel, planes 1:0
D5:4	2nd pixel
D3:2	3rd pixel
D1:0	Right-most pixel
	display four pixels, left to right
V1: 1-BIT (MONOCHROME OR 2-COLOR)	
D31:24	XXXX XXXX
D23:16	XXXX XXXX
D15:8	XXXX XXXX
D7	Left-most pixel
D6	2nd pixel
⇓	⇓
D0	Right-most pixel
	display eight pixels, left to right

TABLE 26-2. DISPLAY MEMORY PIXEL FORMATS

BITS	FUNCTION
	C16: 16-BIT TEXT (16-COLOR)
D0	1st (left-most) pixel of character
⇓	⇓
D7	8th pixel of character(1)
D10:8	Foreground color, bits 2:0
D11	Font(2) / Foreground color, bit 3
D14:12	Background color, bits 2:0
D15	Blink / Background color, bit 3
	display eight or nine pixels of this character
	I4: 4-BIT INDEXED (16-COLOR)
D3:0	Left pixel, indexed color (1 of 16)
D7:4	Right pixel, indexed color (1 of 16)
	display both pixels, first left then right
	I8: 8-BIT INDEXED (256-COLOR)
D7:0	Indexed color (1 of 256)
	DI8: 8-BIT DIRECT INDEX
D1:0	Blue color (1 of 4)
D4:2	Green color (1 of 8)
D7:5	Red color (1 of 8)
	D8: 8-BIT DIRECT COLOR
D1:0	Blue level (0-3)
D4:2	Green level (0-7)
D7:5	Red level (0-7)
	D15: 15-BIT DIRECT (32K-COLOR)
D4:0	Blue level (0-31)
D9:5	Green level (0-31)
D14:10	Red level (0-31)
D15	this bit is a 0 in the desktop window and a 1 in the inset window
	D16: 16-BIT DIRECT (65K-COLOR)
D4:0	Blue level (0-31)
D10:5	Green level (0-63)
D15:11	Red level (0-31)
	D24: 24-BIT DIRECT (2M COLOR)
D7:0	Blue level (0-255)
D15:8	Green level (0-255)
D23:16	Red level (0-255)

TABLE 26-2. DISPLAY MEMORY PIXEL FORMATS (Continued)

BITS	FUNCTION				
YUV8: 8-BIT STRETCHED YUV					
D7:0	Y, luminance level (1-254), or				
	00h, repeat last Y value, or				
	U, chrominance value (0-254), or				
	V, chrominance value (0-254), or				
	FFh, synchronization code (expect Y next)				
YUV12: 12-BIT YUV 4:1:1					
D7:0	Y0[7:0]	Y1[7:0]	Y2[7:0]	Y3[7:0]	Luminance
D9:8	V0-3[7:6]	V0-3[5:4]	V0-3[3:2]	V0-3[1:0]	Chrominance
D11:10	U0-3[7:6]	U0-3[5:4]	U0-3[3:2]	U0-3[1:0]	Chrominance
D14:12	x	---	---	---	---
D15	1	1	1	1	---
YUV15: 15-BIT STRETCHED YUV					
D7:0	Y, luminance level (1-254)				
D12:8	U7:3, upper 5 bits of chrominance, or				
	V7:3, upper 5 bits of chrominance, or				
	U and V (if D14=1)				
D14:13	00 (if D12:8 contains U7:3), or				
	01 (if D12:8 contains V7:3), or				
	1X (if D13:11 contains V2:0 and D10:8 contains U2:0)				
D15	1				
YUV16: 16-BIT STRETCHED YUV					
D7:0	Y, luminance level (1-254), or				
	00h, repeat last Y value, or				
	FFh, synchronization code (expect YU next)				
D15:8	U, chrominance value (0-254), or				
	V, chrominance value (0-254), or				
	X				
Y8: 8-BIT STRETCHED Y					
D7:0	Y, luminance level (1-254)				

NOTES:

(1) For 9-dot fonts, the ninth pixel is either 0 or a copy of eighth pixel.
(2) Selects between two 256-character fonts.
(3) The color selected by all ones is reserved for transparency.
(4) The color selected by all zeros is reserved for auto-repeat.

TABLE 26-2. DISPLAY MEMORY PIXEL FORMATS (Continued)

26.3 DISPLAY MEMORY YUV FORMATS

The display memory YUV formats are listed in Table 26-3.

NOTE

In this example, a 4:2:2 YUV is pixel stretched such that the first pixel (Y1) is displayed four times and the second pixel ("Y2") is displayed three times, for a total of seven pixels. Y3 represents the first pixel of the next group. In a 4:1:1 YUV8, a new group is signaled by the fourth non-zero value after V.

CURRENT STRETCHED 4:2:2 GROUP								NEXT
ACTUAL YUV VALUES								
Y	**Y1**	**Y1**	**Y1**	**Y1**	**Y2**	**Y2**	**Y2**	**Y3**
U	U	U	U	U	U	U	U	U
V	V	V	V	V	V	V	V	V
YUV16								
D7:0(1)	Y1	00(2)	00	00	Y2	00	00	Y3(3)
D15:8	U	V	x	x	x	x	x	U
YUV8								
D7:0(1)	Y1(4)	U	V	00(2)	00	Y2(4)	00	Y3(5)
YUV15								
D7:0	Y1	Y1	Y1	Y1	Y2	Y2	Y2	Y3
D12:8	U7:3	V7:3	---	U7:3	V7:3	---	U7:3	U7:3
D10:8	---	U2:0	---	---	U2:0	---	---	---
D13:11	---	V2:0	---	---	V2:0	---	---	---
D14:13	00	01	1-	00	01	1-	00	00
D15	1	1	1	1	1	1	1	1
Y8								
D7:0	Y1	Y1	Y1	Y1	Y2	Y2	Y2	Y3

NOTES:

(1) A value of FFh in any pixel is a synchronization code causing a Y1 pixel to be expected next.
(2) The value of 00 repeats the last Y.
(3) A new group is signaled by second non-zero value after Y1.
(4) This pixel is displayed twice.
(5) A new group is signaled by the second non-zero value after V.

TABLE 26-3. STRETCHED YUV FORMATS

27.0 OPERATING ENVIRONMENT

The following table lists the absolute maximum ratings for the WD9710 controller.

Ambient Operating Temperature Range under Bias	0°C to 70°C, 32°F to 158°F
Storage Temperature Range	-40°C to 125°C, -40°F to 257°F
Voltage on any Input or Output Pin with respect to V_{SS}	-0.3 to 6.3 Volts
Dynamic Power Dissipation	**To be determined**
Static Power Dissipation (with CRTC refresh turned off)	**To be determined**
Electrostatic Discharge	2000 Volts Human Body Model

TABLE 27-1. ABSOLUTE MAXIMUM RATINGS

CAUTION

Stresses above those listed in the table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

28.0 INTERNAL DAC SPECIFICATIONS

Table 28-1 lists the specifications for the RED, GREEN, and BLUE DACs from the internal RAMDAC of the WD9710 controller.

PARAMETER	MIN	TYP	MAX	CONDITIONS
DAC Resolution	8 Bits per Output			
Integral Linearity Error			± 1 LSB	Least Squares Fit
Differential Linearity Error			± 1 LSB	Least Squares Fit
White Level	17.73 mA	18.6 mA	19.59 mA	VREF = 1.235V, RSET = 8.45K Ohm
Black Level	-20 µA		+20 µA	
LSB Size		73.2 µA		V_{REF} = 1.235V, R_{SET} = 8.45K Ohm
Gray Scale Error			5%	
Glitch Energy			50 pJ	
Settling Time			12 ns	100 pF Load
DAC to DAC Matching			5%	
Output Compliance Current Tolerance	-5%		+5%	
Voltage Reference (VREF) Range	1.14V	1.235V	1.26V	**NOTE:** Do not ground the VREF input pin at any time.
Voltage Reference Input Current (VREF) Refer to NOTE			10 µA	
RSET Value, FSADJ Input		8.45K		37.5 ohm Load
Input Current, $\overline{MDET}$			10 µA	External RAMDAC Mode

TABLE 28-1. DAC SPECIFICATIONS

29.0 DC ELECTRICAL SPECIFICATIONS

29.1 STANDARD OPERATING CONDITIONS

The characteristics listed in the following tables apply to standard operating conditions, unless otherwise noted. All voltages are referenced to VSS (0V Ground). Positive current flows into the referenced pin. The standard operating voltage range is 4.75 to 5.25 VDC

29.2 DC CHARACTERISTICS

The DC voltage characteristics for active signal pins of the WD9710 controller are listed in Table 29-1. The table lists signals names for the PCI bus configuration so that each DC signal pin is accounted for.

The minimum and maximum voltage, current, and capacitance for each pin are listed in Table 29-2.

SIGNAL NAMES	SIGNAL TYPE(1)	SOURCE/ SINK (mA)
$\overline{\text{FRAME}}$, C/$\overline{\text{BE3:0}}$	TTL, Hys, pu	---
$\overline{\text{CHIPKILL}}$, $\overline{\text{IRDY}}$, $\overline{\text{RST}}$, CLK	TTL	---
MCLK, VCLK, CLKI	TTL, Schmitt	---
$\overline{\text{DEVSEL}}$, IRQ	TTL, Tri	16
HSYNC, VSYNC	TTL, Tri	8
AD31:0	TTL, Hys, pu	8
$\overline{\text{EBROM}}$	TTL, Tri	2
MA9:0, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{CAS7:0}}$, $\overline{\text{RAS1:0}}$	CMOS, Tri	16
MD63:0	CMOS, Tri, pu	8
$\overline{\text{RPLT}}$, $\overline{\text{WPLT}}$, $\overline{\text{EXVID}}$, $\overline{\text{BLANK}}$, $\overline{\text{EXVID}}$, $\overline{\text{PCLK}}$, PAR, IDSEL, D21(3), WCLK, $\overline{\text{EXPCLK}}$, $\overline{\text{EXSYNC}}$, VID12:0, USR4, 3, 0	TTL	8
USR2:1	TTL, Tri	8
$\overline{\text{STOP}}$, $\overline{\text{TRDY}}$	TTL, Hys, pu	16(2)

NOTES:

(1) Signal type lists abbreviations for characteristics that are operational to the particular signal as follows:

Abbreviation	Description
TTL	Transistor-to-Transistor Logic
CMOS	Complementary Metal Oxide Semiconductor
Hys	300 mV Hysteresis
Tri	Tristate
pu	50K to 150K pull up resistor

(2) This value specifies sink current only.

(3) This signal (D21) is de-multiplexed VL-bus signal, which is listed here because the PCI bus does not use the applicable connector pin (123).

TABLE 29-1. DC SIGNAL CHARACTERISTICS

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS	CONDITIONS	APPLIES TO SIGNAL NAMES
V_{IL}	TTL Input Low Voltage	-0.3	0.8	V		AD31:0, AEN, BALE, SBHE, EMEM, EXVID, IOCS16, IOR, IOW, MDET, MEMR, MEMW, RSET
V_{IH}	TTL Input High Voltage	2.0	VCC + 0.3	V	VCC = 5V +/- 5%	
I_{IL}	Input Low Current	---	+/- 10	µA	VIN = 0.0V	BALE, EMEM, IOCS16, IOR, IOW, MCLK, MEMR, MEMW, RSET
I_{IH}	Input High Current	---	+/- 10	µA	VIN = VCC	
V_{OL}	TTL Output Low Voltage	---	0.4	V	IOL = Rated Current from Table 29-1.	BLANK, BUFDIR, EABUF, EBROM, EDBUF, HSYNC, IOCHRDY, IRQ, MEMCS16, PCLK, RPLT, USR1:0, VID15:0, VSYNC, WPLT, V_{OL} only for: IOCS16, SRDY
V_{OH}	TTL Output High Voltage	2 4	---	V	IOH = Rated Current from Table 29-1.	
V_{CL}	CMOS Input Low Voltage	-0 3	1.0	V		CAS7:0, MCLK, MD63:0, VCLK, LCLK V_{CL} only for: SRDY, IOCS16
V_{CH}	CMOS Input High Voltage	VCC-1 0	VCC +0.3	V	VCC = 5V +/- 5%	
V_{COL}	CMOS Output Low Voltage	---	0.5	V	ICOL = Rated Current from Table 29-1.	CAS7:0, MA9:0, MD63:0, RAS1:0, WE
V_{COH}	CMOS Output High Voltage	VCC -0 5	---	V	ICOH = Rated Current from Table 29-1.	
I_{PL}	Pull-up Input Low Current	-10	-110	µA	50K TO 150K Internal Pull-up Resistor	AD30:0, SBHE, EXVID, MD63:0, MDET, VCLK
I_{PH}	Pull-up Input High Current	---	+/- 10	µA		
I_{OZ}	High Impedance Leakage Current	-10 0	10.0	µA	0V < VOUT < VCC	
C_{IN}	Input Capacitance	--	10	pF	FC = 1 MHz	
C_{OUT}	Output Capacitance	---	10	pF	FC = 1 MHz	
$C_{I/O}$	I/O Pin Capacitance	---	12	pF	FC = 1 MHz	

TABLE 29-2. DC POWER CHARACTERISTICS

30.0 AC TIMING CHARACTERISTICS

NOTE

AC Timing Characteristics are given for example only and do not indicate the actual WD9710 design.

30.1 INTRODUCTION

The following information applies to all of the parameters listed in this section:

- CL = 30 pF unless otherwise noted.
- nt implies n X t, (n times the period t). e.g. 1t, 2t etc.
- #n refers to the number in column 1 of the same table.
- The numbers in the first column of each table are used to locate parameters on the associated diagram.
- Throughout this section, the minimum (MIN) and maximum (MAX) values are given in nanoseconds (ns) unless otherwise specified.

NOTE

Unless otherwise specified, AC timing is with respect to Vil/Vih = 0.4/2.4 and Vol/Voh = 0.8/2.0.

30.2 INTERNAL CLOCK AC CHARACTERISTICS

The following conditions apply to all of the AC parameters presented in this section unless otherwise specified:

- CKIN = 14.31818 MHz
- All units are in nanoseconds (ns) unless otherwise specified.
- Maximum jitter measurements were taken within a range of 30 µs after triggering on a 400 MHz scope.
- Internal CLK rise and fall time between 0.8 and 2.0V at the output of the PCLK.
- External Clock Mode rise and fall time between 0.8 and 2.0V.
- Internal duty cycle measured at 1.4V, at the output of the PCLK.
- External Clock Mode duty cycle measured at 1.4V.

PARAMETER	MINIMUM	MAXIMUM	UNITS
REFERENCE INPUT CLOCK			
Rise Time	---	10	ns
Fall Time	---	10	ns
Phase Jitter	---	1	ns
Duty Cycle	42.5%	57.5%	@1.4V
INTERNAL MCLK AND VCLK TIMING			
Rise Time	---	3	ns
Fall Time	---	3	ns
VCLK Jitter	0	3	ns
MCLK Jitter	0	5	ns
Duty Cycle	45%	65%	@1.4V
Frequency Error	---	0.5%	---
MCLK Frequency Range	45	85	MHz
VCLK Frequency Range	25	135	MHz

TABLE 30-1. CLOCK TIMING CHARACTERISTICS

NO. IN DIAGRAM	PARAMETER	MIN VALUE	MAX VALUE	TEST CONDITIONS
1(1)	VCLK Clock Period	12.5	---	
2	VCLK High	5	-	At 1/2 VDD
3	VCLK Low	5	-	At 1/2 VDD
4(1)	Clock Rise Time	-	2	1V - (VDD - 1V)
5(1)	Clock Fall Time	-	2	1V - (VDD - 1V)
6	VCLK to PCLK Delay	8	20	
7a	VCLK to HSYNC Delay	8	25	
7b	VCLK to VSYNC Delay	8	25	
7c	VCLK to $\overline{\text{BLNK}}$ Delay	8	20	
7d	VCLK to VID7:0 Delay	8	20	
8(2)	MCLK Clock Period	16.6	---	
9	MCLK High	8		At 1/2 VDD
10	MCLK Low	8		At 1/2 VDD
11	VID15:0 Setup to PCLK	3		
12	VID15:0 Hold from PCLK	3		

NOTES:

(1) Applies to VCLK and MCLK.

(2) VCLK and MCLK use CMOS level input buffers. V(IL) maximum = 1.5V, V(IH) minimum = VDD - 1.5V

TABLE 30-2. CLOCK TIMING

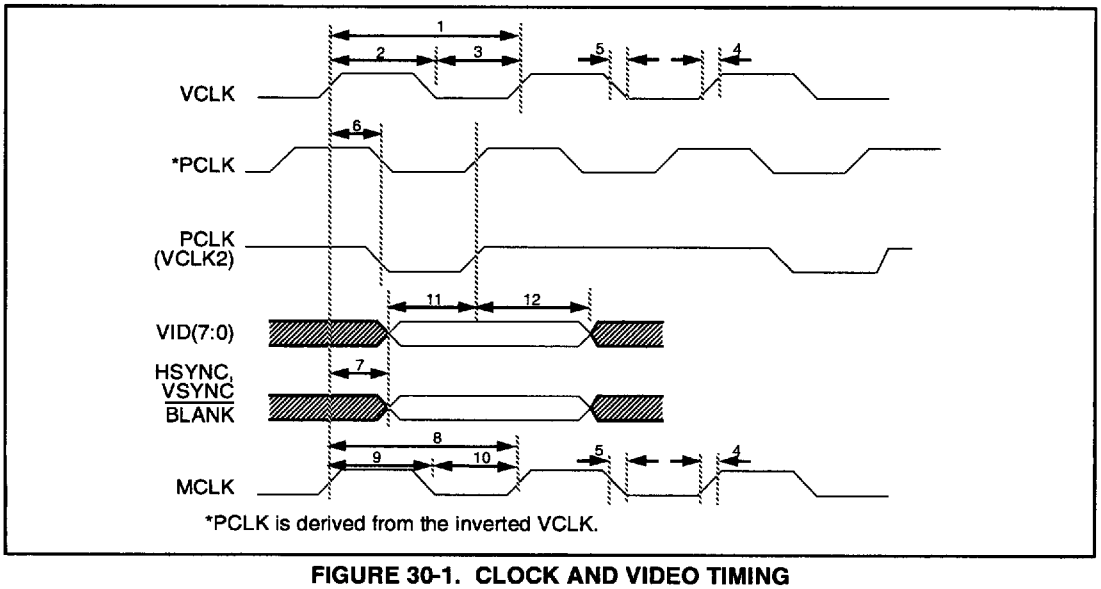

FIGURE 30-1. CLOCK AND VIDEO TIMING

NO. ON DIAGRAM	PARAMETER	MIN VALUE	MAX VALUE	TEST CONDITIONS
1	RESET Pulse Width	10t	-	t = 1/MCLK (For configuration at Power-0n and Reset)
2	MD/AD setup to RESET Low	50	-	
3	MD/AD Hold from RESET Low	30	-	
4	RESET Low to First $\overline{IOW}$	10t	-	

TABLE 30-3. RESET TIMING

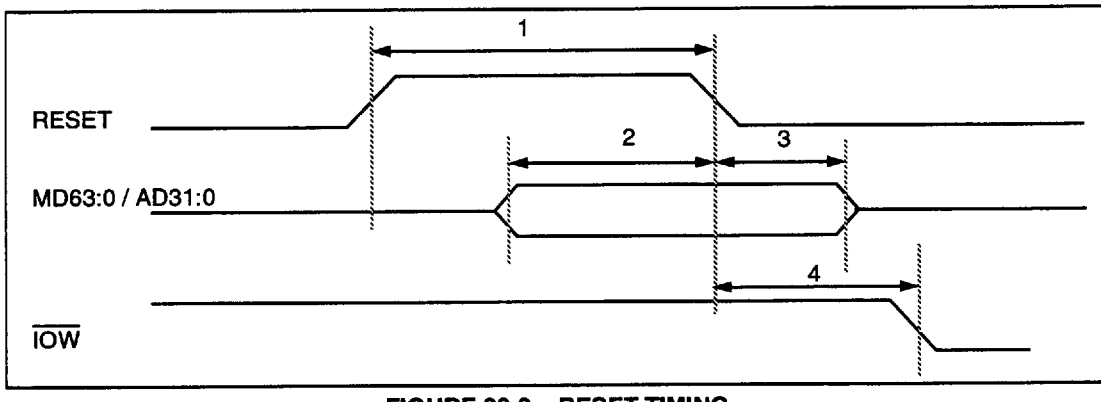

FIGURE 30-2. RESET TIMING

NO. IN DIAGRAM	PARAMETER	MIN (ns)	MAX (ns)	COMMENTS
1	LCLK Period	25	--	1.4V Threshold
2	LCLK Low Time	10	--	1.4V Threshold
3	LCLK High Time	10	--	1.4V Threshold
3a	LCLK Fall Time	--	3	2.4V to 0.8V
3b	LCLK Rise Time	--	3	0.8V to 2.4V
4	AD31:0, $\overline{BE}$3:0, M/$\overline{IO}$, to $\overline{LDEV}$	5	20	CL = 100 pF
5	AD31:0, $\overline{BE}$3:0, M/$\overline{IO}$, W/$\overline{R}$, $\overline{ADS}$ Setup to LCLK	7	--	One Wait State
6	AD31:0, $\overline{BE}$3:0, M/$\overline{IO}$, W/$\overline{R}$, $\overline{ADS}$ Hold From LCLK	13	--	Zero Wait State
7	LCLK to AD31:0 Out	3	14	CL = 100 pF
8	LCLK to AD31:0 Tristate	3	19	CL = 100 pF
9	LCLK to $\overline{ADS}$ Low to $\overline{LRDY}$ Low	c*t+5	2.5 µs	t = LCLK Period c = Setting of xxxxh, Bit 6 CL = 100 pF
10	$\overline{LRDY}$ Low to $\overline{LRDY}$ High	t+2	t+10	
11	LCLK to $\overline{LRDY}$ Hi-Z	3	20	
12	AD31:0 in Setup Before LCLK	11	--	
13	AD31:0 Hold After LCLK	5	--	
14	RDYRTN to LCLK before $\overline{ADS}$ Setup	7	---	
15	LCLK to RDYRTN hold	3	---	
16	LCLK to $\overline{VGARDY}$ Low	2	14	CL = 100 pF
17	AD31:0, $\overline{BE}$3:0, M/$\overline{IO}$, to EPROM Low	5	35	xxxx0h, Bit 7 = 0 External BIOS

TABLE 30-4. MULTIPLEXED VL-BUS INTERFACE TIMING

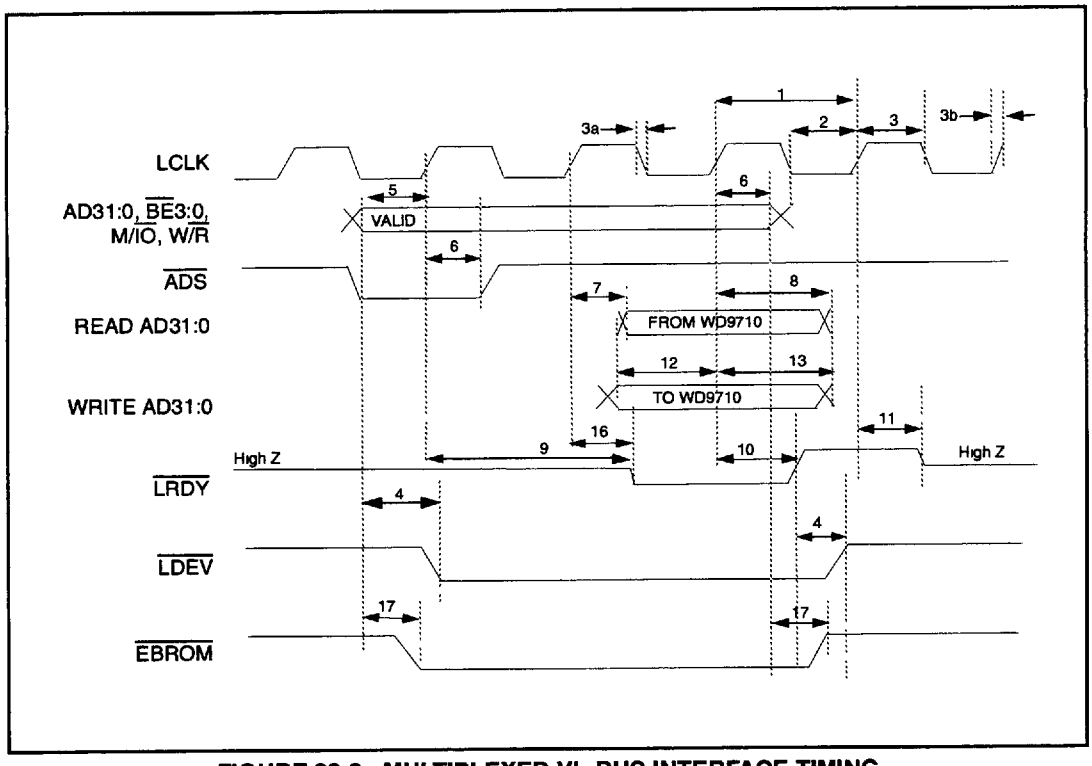

FIGURE 30-3. MULTIPLEXED VL-BUS INTERFACE TIMING

NO. IN DIAGRAM	PARAMETER	MIN (ns)	MAX (ns)	COMMENTS
1	LCLK Period	25	--	1.4V Threshold
2	LCLK Low Time	10	--	1.4V Threshold
3	LCLK High Time	10	--	1.4V Threshold
3a	LCLK Fall Time	--	3	2.4V to 0.8V+
3b	LCLK Rise Time	--	3	0.8V to 2.4V
4	AD23:2, $\overline{ADRM}$, $\overline{ADRZ}$, $\overline{BE}$3:0, M/$\overline{IO}$, to $\overline{LDEV}$	5	20	CL = 100 pF
5	AD23:2, $\overline{ADRM}$, $\overline{ADRZ}$, $\overline{BE}$3:0, M/$\overline{IO}$, W/$\overline{R}$, $\overline{ADS}$ Setup to LCLK	7	--	One Wait State
6	AD23:2, $\overline{ADRM}$, $\overline{ADRZ}$, $\overline{BE}$3:0, M/$\overline{IO}$, W/$\overline{R}$, $\overline{ADS}$ Hold From LCLK	13	--	Zero Wait State
7	LCLK to DAT23:0 Out	3	14	CL = 100 pF
8	LCLK to DAT23:0 Tristate	3	19	CL = 100 pF
9	LCLK to $\overline{ADS}$ Low to $\overline{LRDY}$ Low	c*t+5	2.5 µs	t = LCLK Period c = Setting of xxxxh, Bit 6 CL = 100 pF
10	$\overline{LRDY}$ Low to $\overline{LRDY}$ High	t+2	t+10	
11	LCLK to $\overline{LRDY}$ Hi-Z	3	20	
12	DAT23:0 in Setup Before LCLK	11	--	
13	DAT23:0 Hold After LCLK	5	--	
14	RDYRTN to LCLK before $\overline{ADS}$ Setup	7	---	
15	LCLK to RDYRTN hold	3	---	
16	LCLK to $\overline{LRDY}$ Low	2	14	CL = 100 pF
17	AD23:2, $\overline{ADRM}$, $\overline{ADRZ}$, $\overline{BE}$3:0, M/$\overline{IO}$ to EPROM	5	35	xxxxh, Bit 7 = 0 External BIOS

TABLE 30-5. DE-MULTIPLEXED VL-BUS INTERFACE TIMING

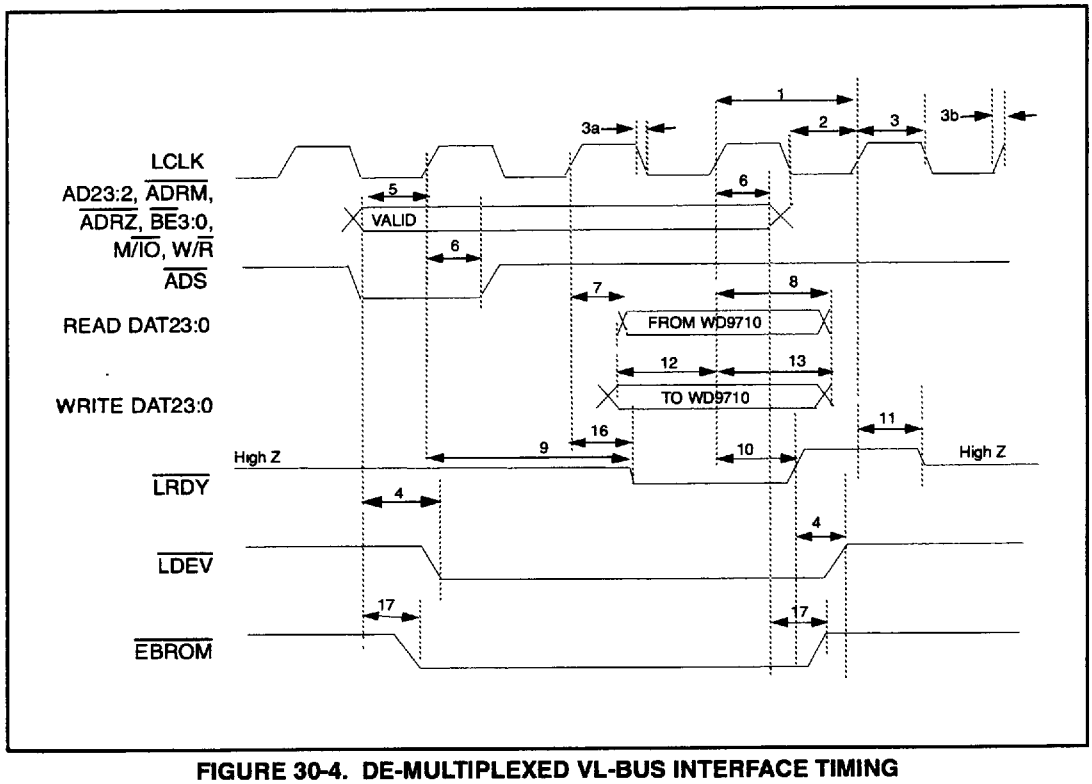

FIGURE 30-4. DE-MULTIPLEXED VL-BUS INTERFACE TIMING

NO. ON DIAGRAM	PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	TEST CONDITIONS
1	AD23:0 Valid to $\overline{RPTL}$ or $\overline{WPTL}$ Low	t - 4	-	t = LCLK Cycle Time
2	$\overline{RPTL}$ or $\overline{WPTL}$ Low Time	n * t - 15	n * t	t = LCLK Cycle Time n based on 2DE0h, Bit 4 as follows: Bit 4 = 0 then n = 9 Bit 4 = 1 then n = 18
3	Read VID15:0 Setup to LCLK	10	-	These times apply to EPROM also.
4	Read VID15:0 Hold After LCLK	10	-	
5	LCLK rise to $\overline{RPTL}$ or $\overline{WPTL}$	3	22	
6	$\overline{WPTL}$ rise to VID15:0 hold	10	-	
7	VID15:0 setup to $\overline{WPLT}$ rise	10		

TABLE 30-6. EXTERNAL RAMDAC TIMING

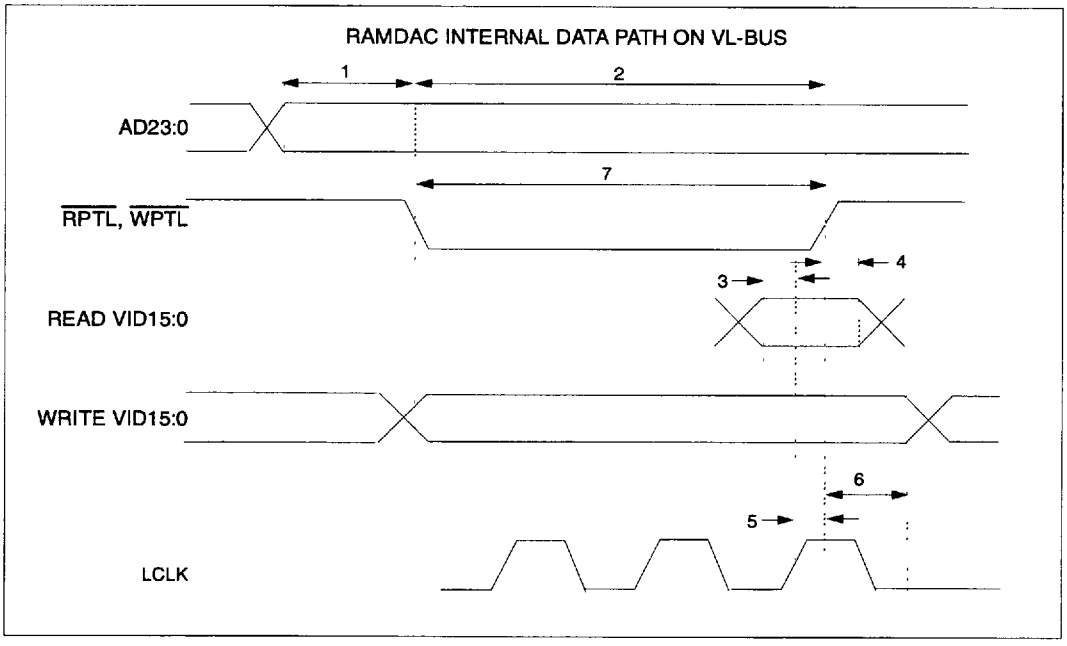

FIGURE 30-5. EXTERNAL RAMDAC TIMING

NO. ON DIAGRAM	PARAMETER	MINIMUM VALUE	MAXIMUM VALUE	TEST CONDITIONS
1	$\overline{RAS}$1:0 Cycle Time	6t	-	Note 2, 3
2	$\overline{RAS}$1:0 Pulse Width Low	3.5t - 7	-	Note 2, 3
3	$\overline{RAS}$1:0 High Time (Precharge)	2.5t + 2	-	Note 2, 3
4	$\overline{RAS}$1:0 Low to $\overline{CAS}$ Low	2.5t - 9	2.5t - 4	Note 2, 3
5	$\overline{CAS}$7:0 Cycle Time	2t	-	Note 3
6	$\overline{CAS}$7:0 Pulse Width Low	1t + 2	-	Note 2, 3
7	$\overline{CAS}$7:0 High Time (Precharge)	1t - 7	-	Note 2, 3
8	Row Address Setup to $\overline{RAS}$1:0 Low	1t - 10	-	Note 3
9	Row Address Hold Time from $\overline{RAS}$1:0 Low	1t - 8	-	Note 3
10	Column Address Setup to $\overline{CAS}$7:0 Low	1t - 5	-	Note 3
11	Column Address Hold from $\overline{CAS}$7:0 Low	1t - 4	-	Note 3
12	Read Data Valid Before $\overline{CAS}$7:0 High	2	-	
13	Read Data Hold After $\overline{CAS}$7:0 High	0	-	
14	Write Data Setup to $\overline{CAS}$7:0 Low	1t - 15	-	Note 3
15	Write Data Hold After $\overline{CAS}$7:0 Low	1t - 5	-	Note 3
16	$\overline{WE}$ Low Setup to $\overline{CAS}$7:0 Low	1t - 5	1t + 5	Note 3
17	$\overline{WE}$ Low Hold After $\overline{CAS}$7:0 High	1t - 5	1t + 9	Note 5
18	$\overline{OE}$ High Before $\overline{WE}$ Low	-2	-	Note 3
19	$\overline{OE}$ Low After $\overline{WE}$ High	0	-	Note 3
20	$\overline{CAS}$7:0 High for $\overline{CAS}$ Before $\overline{RAS}$1:0 Refresh	1t - 10	-	Note 3
21	$\overline{RAS}$1:0 Low from $\overline{CAS}$7:0 Low for $\overline{CAS}$ before $\overline{RAS}$ Refresh	0.5t + 4	-	Note 3

NOTES:

(1) The timing in this table results from setting 3C5h, Index 13 to XXX00000b.

(2) This timing is adjustable via 3C5h Index 13 (see Figure 30-7.

(3) For t = 1/MCLK, the maximum MCLK frequency is:

DRAM SPEED	FREQUENCY
70 ns	44.7 MHz
60 ns	49.5 MHz
45 ns	60.0 MHz

(4) Numbers the first column correspond to numbers on the timing diagram Figure 30-6.

(5) Memory write uses fast page early write, while keeping $\overline{OE}$ equal to 1.
Memory read uses fast page read, while keeping $\overline{OE}$ equal to 1.

TABLE 30-7. DRAM TIMING FOR 256K BY 16 DRAMS

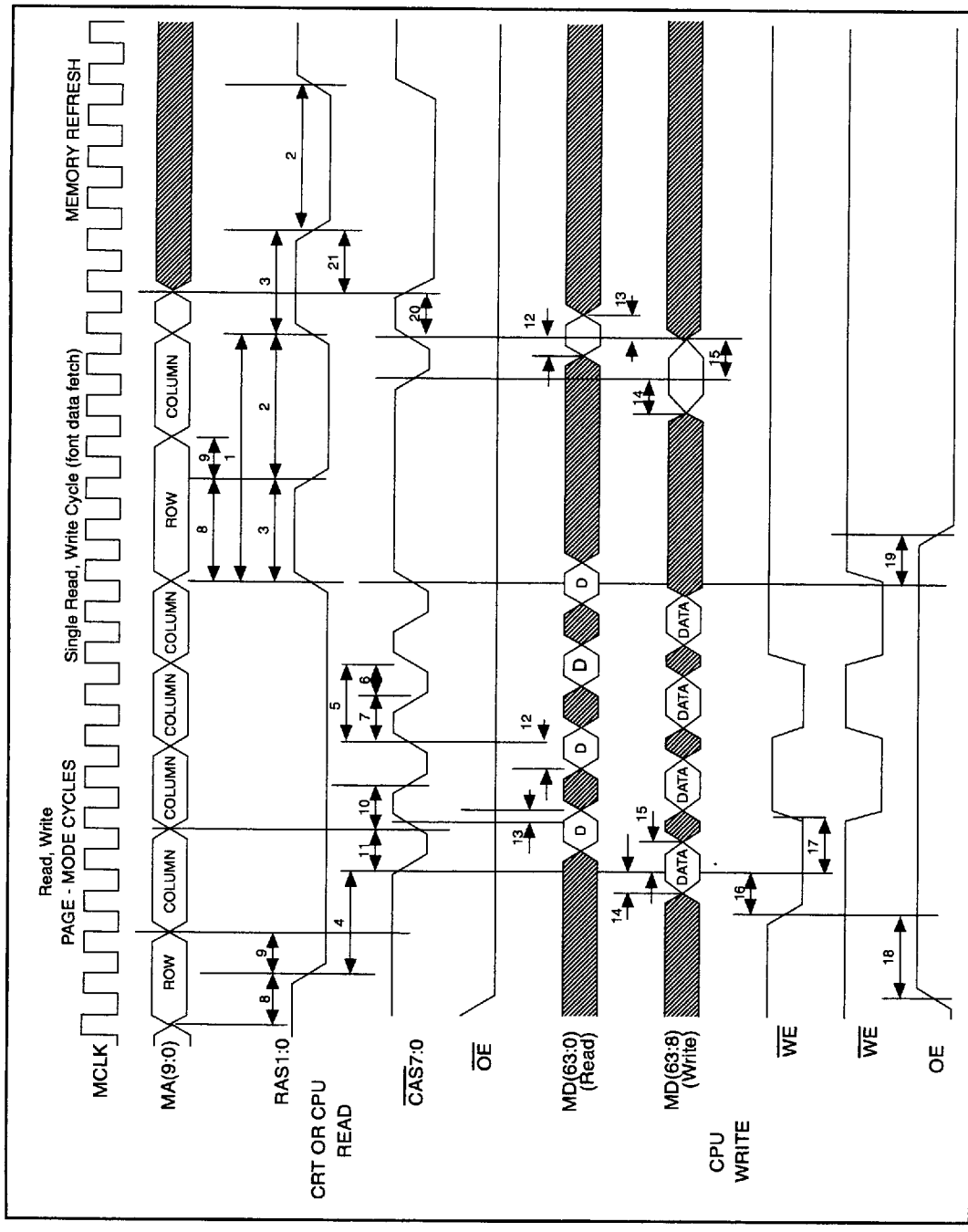

FIGURE 30-6. DRAM TIMING

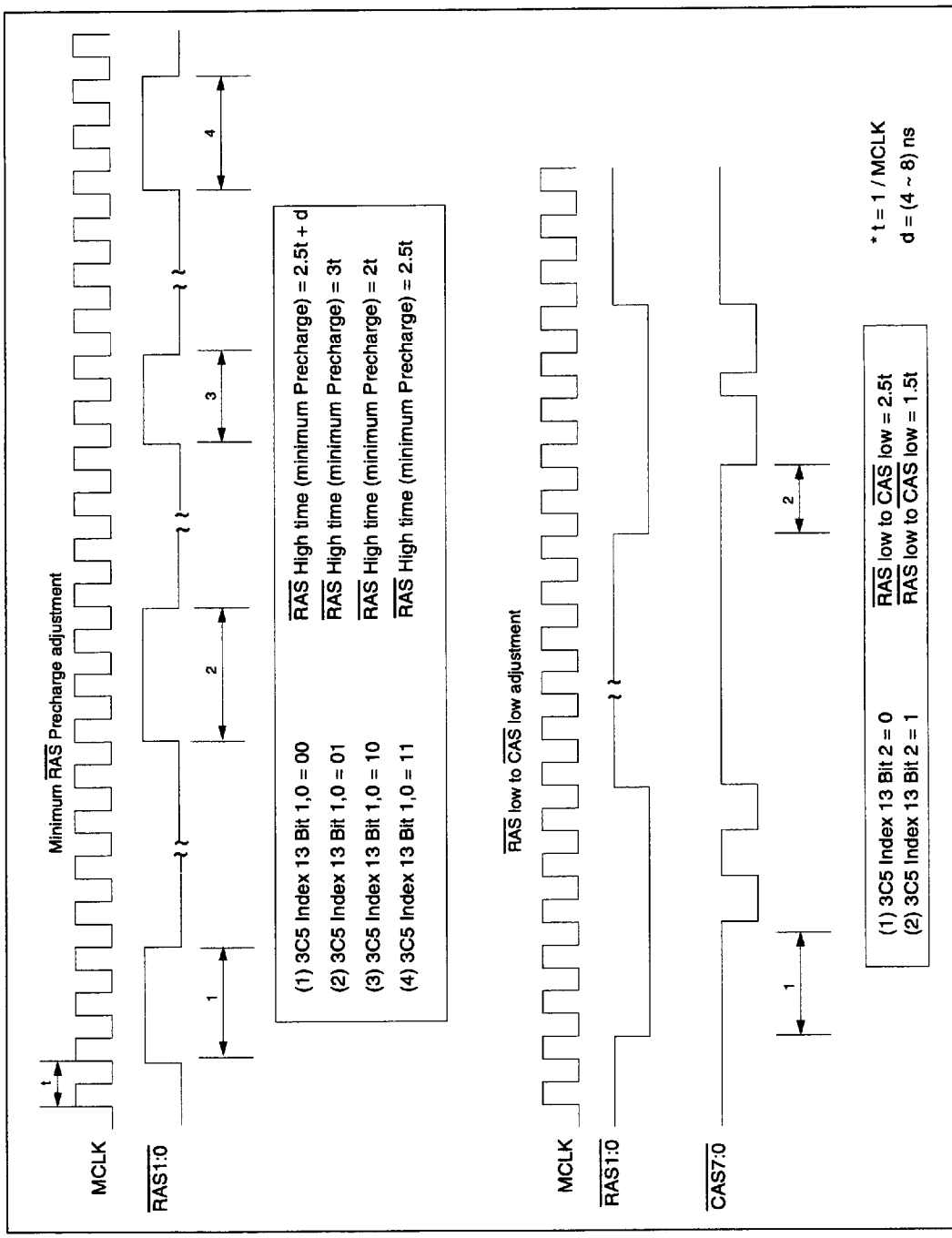

FIGURE 30-7. DRAM TIMING ADJUSTMENT

30.3 DRAM TIMING ADJUSTMENT

For DRAM timing adjustments, the $\overline{RAS}$1:0 and $\overline{CAS}$7:0 timing can be adjusted by register 3C5h, Index 13, Bits 4 through 0 (see Figures 30-9 and 30-10.

Table 30-7 lists the parameters that are adjustable via register 3C5h Index 13.

For the CAS pulse width adjustment, the CAS cycle time is always equal to 2t (t = 1/MCLK). The delay "d" is 4 to 7 ns. Therefore, 3C5h Index 13 Bit 3 sets the CAS pulse width as follows:

BIT 3	CAS LOW =	CAS HIGH =
0	1t + (2 ~ 3) ns	1t - (2 ~ 3) ns
1	1t + 2d	1t - 2d

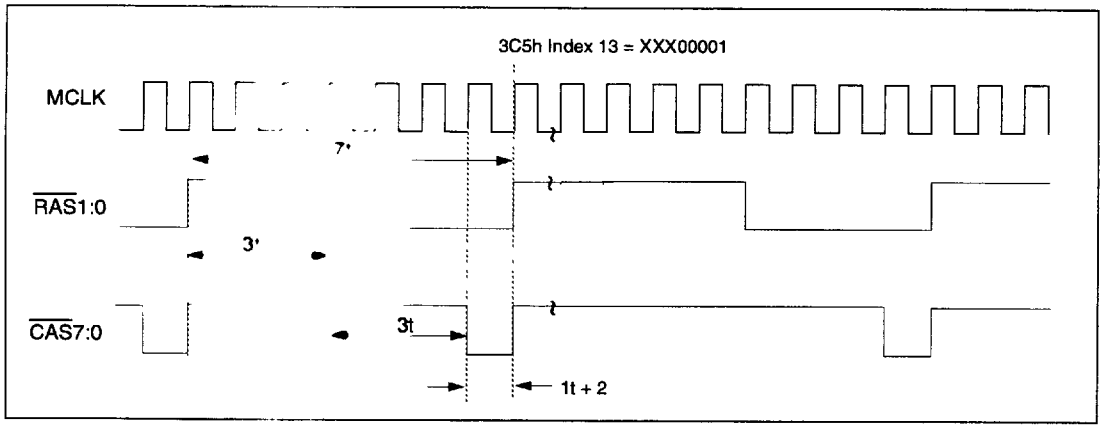

FIGURE 30-8. DRAM TIMING FOR 256K BY 16 DRAM

31.0 PACKAGE DIMENSIONS

Figure 31-1 illustrates the 208-pin MQFP package showing the dimensions in millimeters and inches.

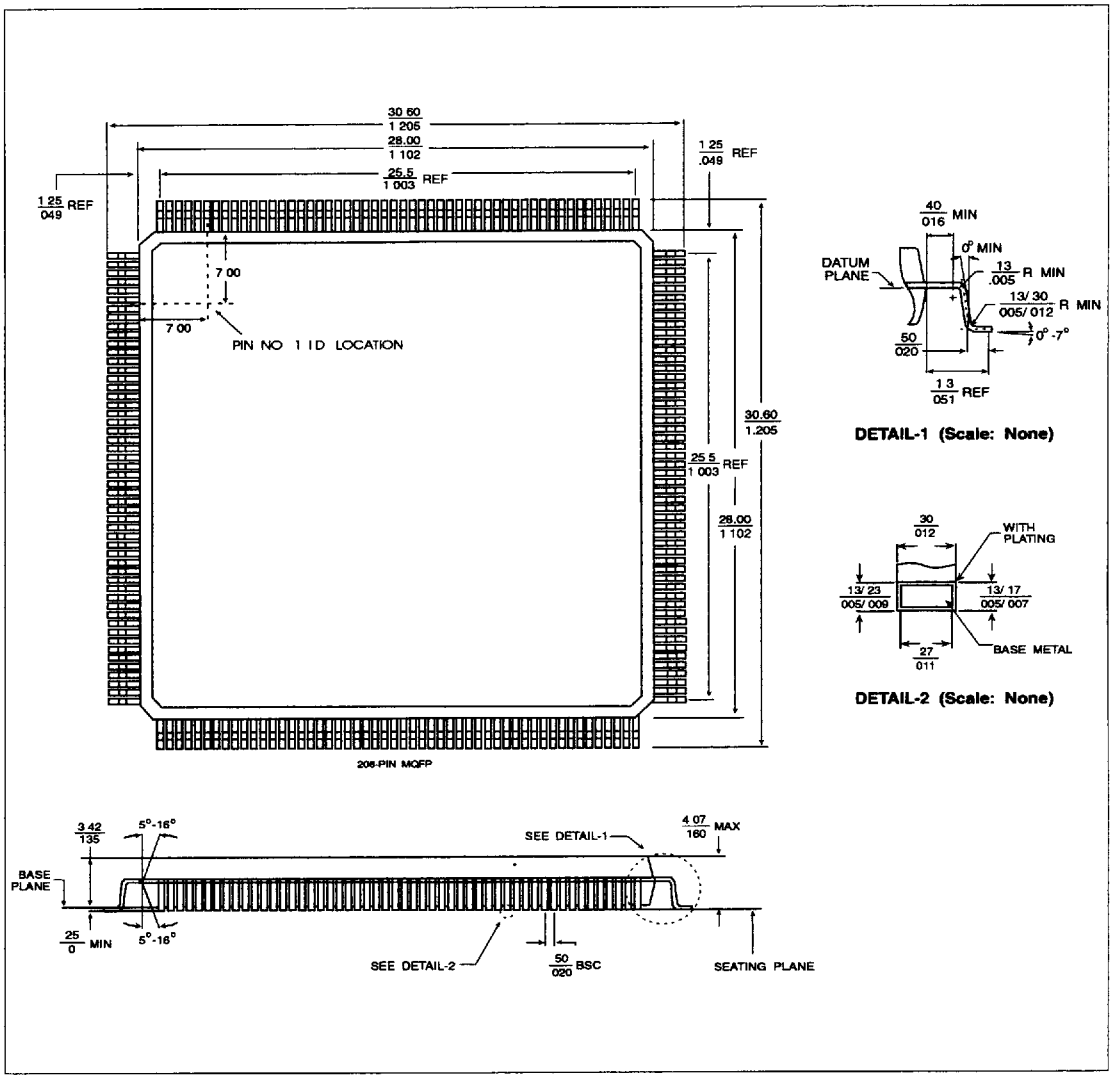

FIGURE 31-1. 208-PIN MQFP PACKAGE DIMENSIONS

A.0 APPENDIX A - REFERENCE DOCUMENTS

For further information on Personal Computer (PC) video display applications, refer to the manuals in the following list.

- IBM PC Hardware User Guide (IBM # 6322510)
- IBM PC XT Hardware User Guide (IBM # 6322511)
- IBM PC AT Hardware User Guide (IBM # 6280066)
- IBM PS/2 Model 30 Hardware User Guide (IBM # 68x2230)
- IBM PC AT Technical Reference Manual (IBM # 6280070)
- IBM PS/2 Model 30 Technical Reference Manual (IBM # 68x2201)
- IBM PC Options & Adapters Technical Reference Manual (IBM # 6322509)
- IBM PS/2 BIOS Reference Manual (IBM # 68x2260)
- IBM PC Reference Manual (IBM # 6025005)
- Hercules Graphics Card Owner's Manual

B.0 APPENDIX B - CHANGE RECORD FOR THE WD9710 DATA BOOK

B.1 SCOPE

This WD9710 Data Book Change Record describes significant changes to the data book since it was last issued. This issue has been updated and replaces the issue dated 11/10/94.

The previous issues of this data book have had limited distribution.

Whenever the data book is reissued, a new change record is generated for that issue and all pages of the issue carry the current issue date. This issue is dated 3/1/95.

B.2 DESCRIPTION OF CHANGES

This issue of the WD9710 Data Book differs in significant ways from the previously published issue. The numbers of the pages that changed since the previous issue are listed in the change record. On each changed page, the changed text is marked by a change bar in the right margin of the text column. Changed figures are marked by a change bar on their title. These change bars will be removed on subsequent issues and new change bars placed by the current changes. On the released version of this data book, all change bars will be removed and the word PRELIMINARY will be removed from the bottom of the page.

Most editorial and typographical corrections are not marked. Also, data that was moved due to additions or deletions are not indicated by change bars.

B.3 CHANGE RECORD

The following table lists the page numbers of pages that were changed since the previous issue date.

CURRENT ISSUE DATE	PREVIOUS ISSUE DATE	PAGES CHANGED SINCE THE PREVIOUS ISSUE
4/12/94	3/4/94	New issue
6/20/94	4/12/94	New issue
11/10/94	6/20/94	1-6, 9-12, 14, 15, 18-26, 28-45, 47-55, 57, 58, 63, 76, 78, 83-86, 91, 92, 94, 95, 101-104, 115, 116, 118, 124, 127, 130, 132, 134, 136-141, 143-152, 155, 158, 171, 172
3/1/95	11/10/94	1-14, 16-19, 22-25, 29-41, 44-46, 48, 49, 51-57, 59-63, 67-74, 76-81, 84, 85 ,88-90, 92-95, 102, 104, 107-120, 124-151, 154, 158, 161, 162

31.0 PACKAGE DIMENSIONS

Figure 31-1 illustrates the 208-pin MQFP package showing the dimensions in millimeters and inches.

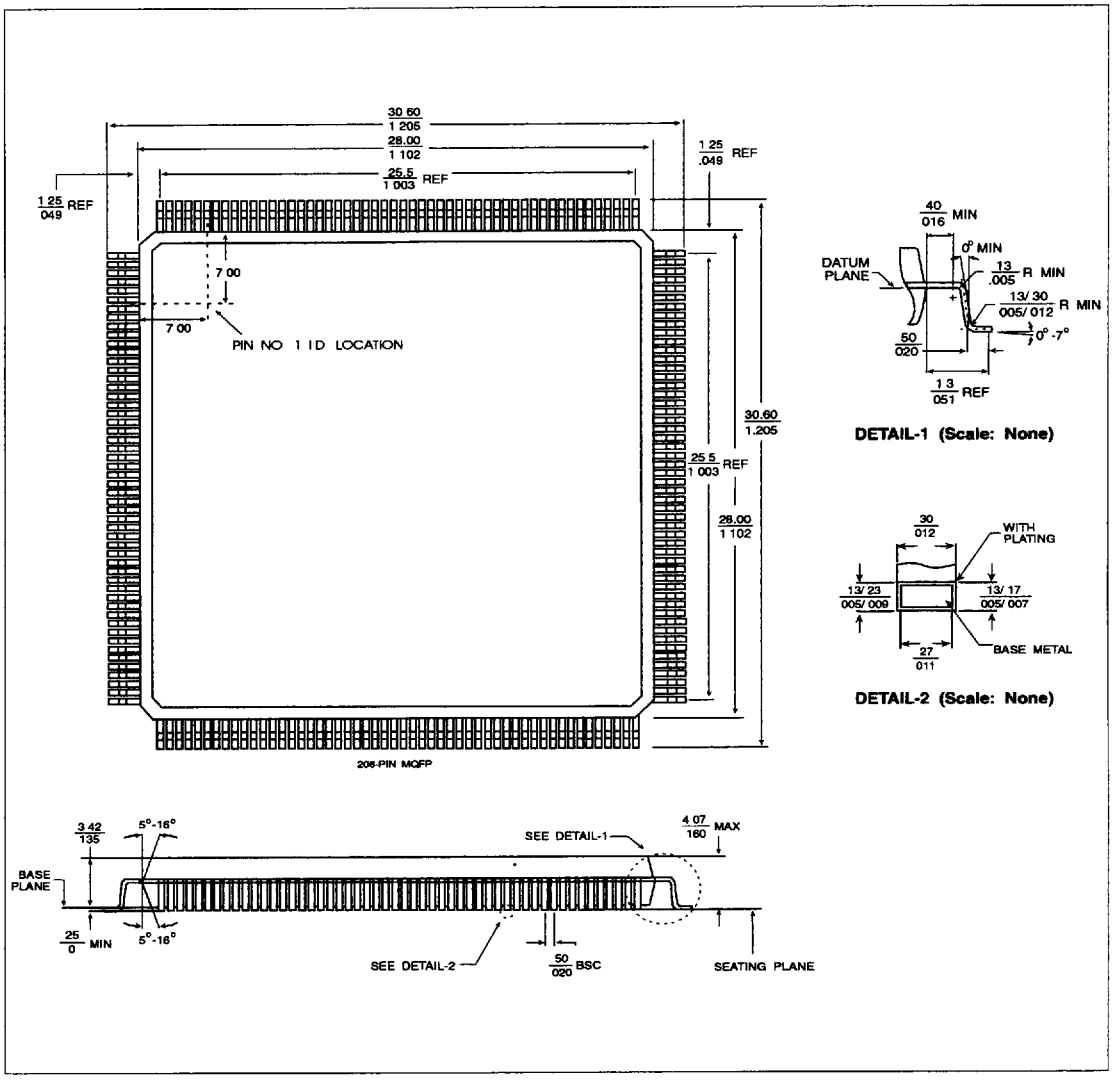

FIGURE 31-1. 208-PIN MQFP PACKAGE DIMENSIONS